

Model Name: GA-P85-D3

2.0

SHEET

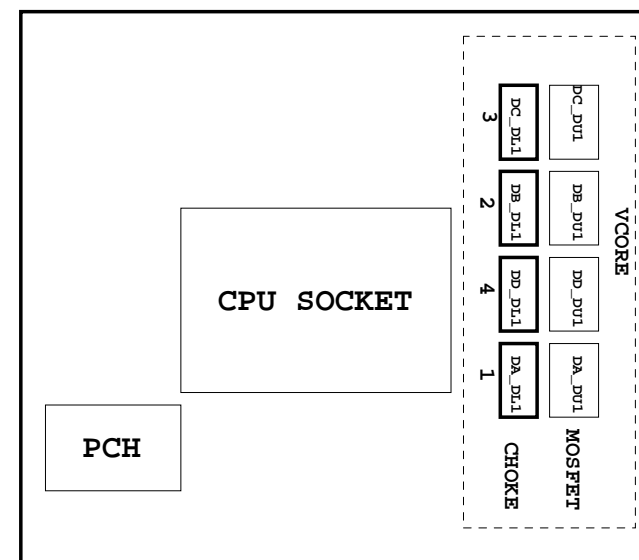
TITLE

01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	CPU_LGA1150-A
05	CPU_LGA1150-B
06	CPU_LGA1150-C
07	DDR III CHANNEL A
08	DDR III CHANNEL B
09	PCH_FDI,DMI,USB,PCIE
10	PCH_RGB,CLK BUFFER
11	PCH_HOST,SATA,PCI
12	PCH_GPIO,CTRL,AUDIO
13	PCH_PWR,GND
14	PCI EXPRESS*16 SLOT
15	PCIEX4 SLOT
16	ITE8892 PCI BRIDGE
17	PCI SLOT 1~4
18	I/O ITE8620
19	COM, -PROHOT, R_USB
20	Dual BIOS / LPT
21	ALC887 CODEC
22	REAR AUDIO JACK
23	VCORE_ ISL95820_1
24	VCORE_ ISL95820_2
25	DDR15V / M3 POWER
26	NCP3933 OVER VOLTAGE
27	DISCRETE POWER

SHEET

TITLE

28	F_PANEL , F_USB2.0/3.0
29	ATX POWER, CLOCK GEN
30	HWM , KB/MS , FAN CTRL
31	Realtek 8111F-VL
32	HDMI
33	TABLE LIST
34	
35	
36	
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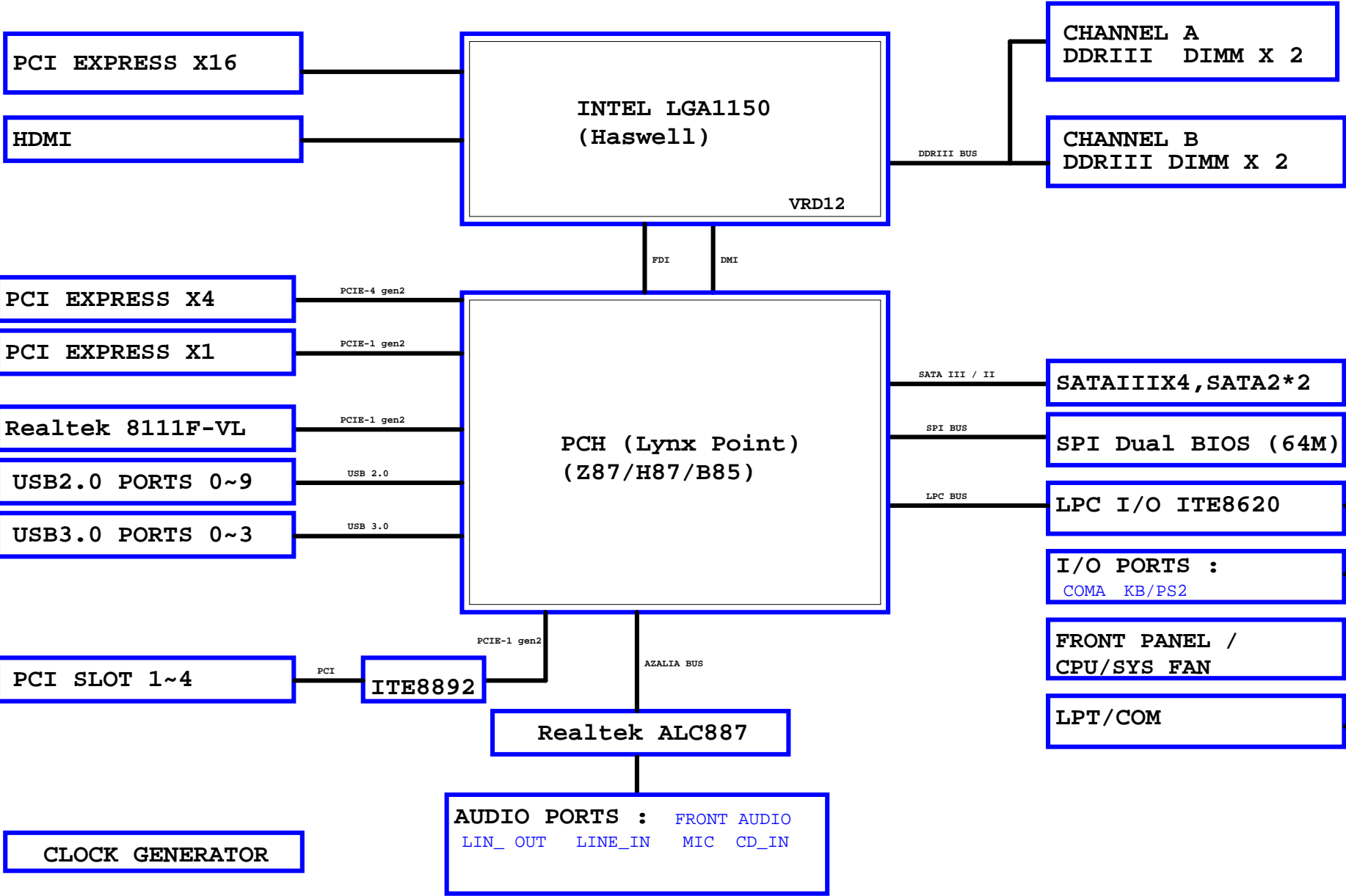


Gigabyte Technology			
Title			
Cover Sheet			
Size	Document Number	GA-P85-D3	Rev
Custom			2.0
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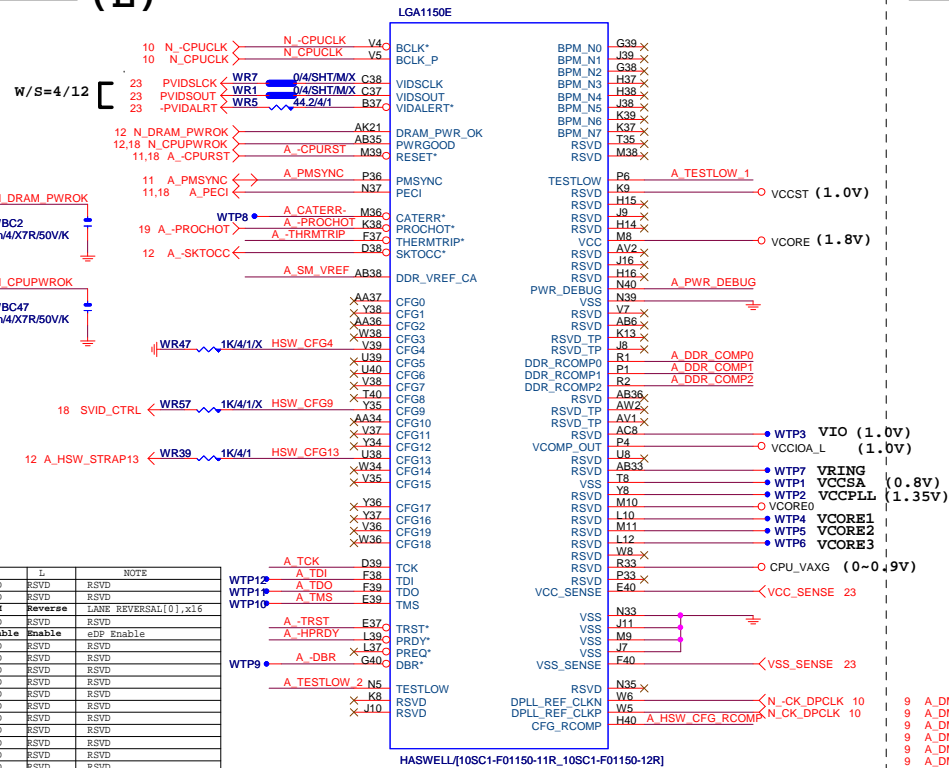
Component value change history

[illegible][illegible]

BLOCK DIAGRAM



LGA1150 (E)

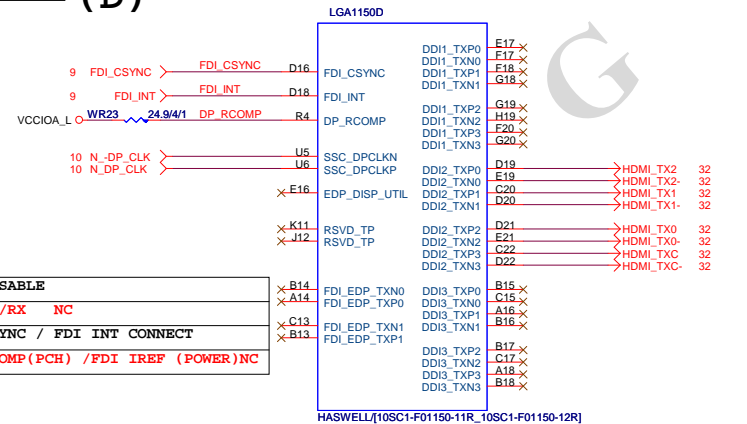


CFG	H	L	NOTE
0	RSVD	RSVD	RSVD
1	RSVD	RSVD	RSVD
2	MORM	Reverse	LANE REVERSAL[0,x]x16
3	RSVD	RSVD	RSVD
4	Disable	Enable	as Enable
7	RSVD	RSVD	RSVD
8	RSVD	RSVD	RSVD
9	RSVD	RSVD	RSVD
10	RSVD	RSVD	RSVD
11	RSVD	RSVD	RSVD
12	RSVD	RSVD	RSVD
13	RSVD	RSVD	RSVD
14	RSVD	RSVD	RSVD
15	RSVD	RSVD	RSVD
16	RSVD	RSVD	RSVD
17	RSVD	RSVD	RSVD

CFG6	CFG5	PCIE CONFIG
1	1	1x16 , Default
1	0	2X8
0	1	RSVD
0	0	X8,X4,X4

CFG 0-17 all internal PULL-UP

LGA1150 (D)



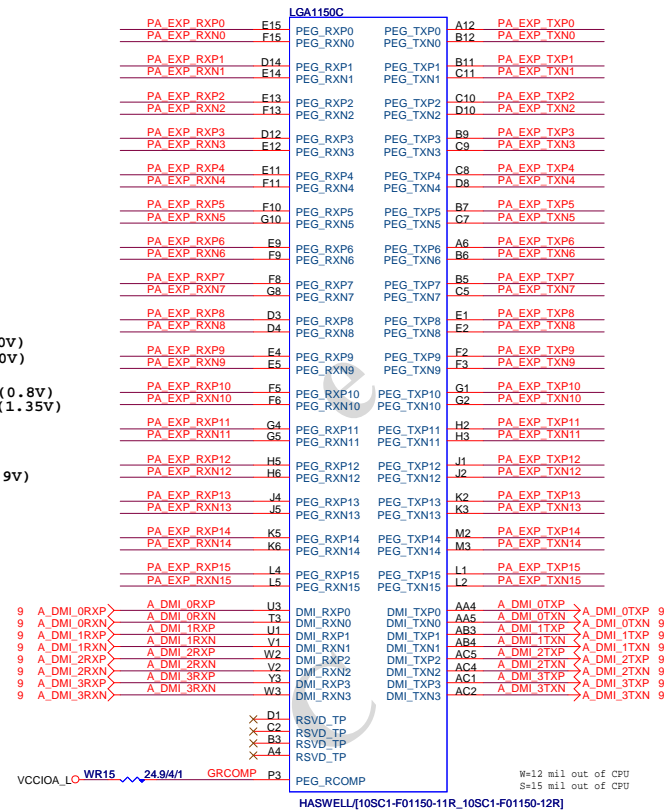
FDI DISABLE
FDI TX/RX NC
FDI CSYNC / FDI INT CONNECT
FDI RCOMP(PCH) /FDI IREF (POWER)NC

FDI:4/4/4//15(breakout min 4/4/4//8)
Impedance=85 +- 15%

DP/HDMI 4/4/4//20 FDI 4/4/4/12

Impedance=85 +- 15%

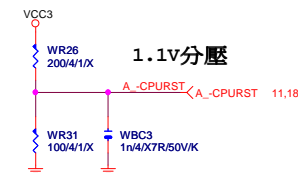
LGA1155 (C)



CPU PEG 5/5/5//20 Impedance=80 +- 15%

DMI 4/4/4//15 Impedance=85 +- 15%

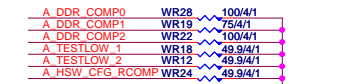
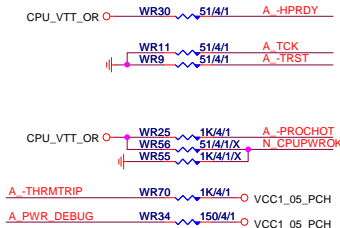
-CPURST



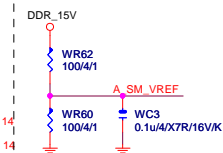
CPU SVID



CPU PU/PD



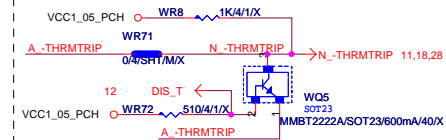
SM REF



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|-----|
|THRMTRIP DISABLE FOR Z87 OVERCLOCK|
|-----|

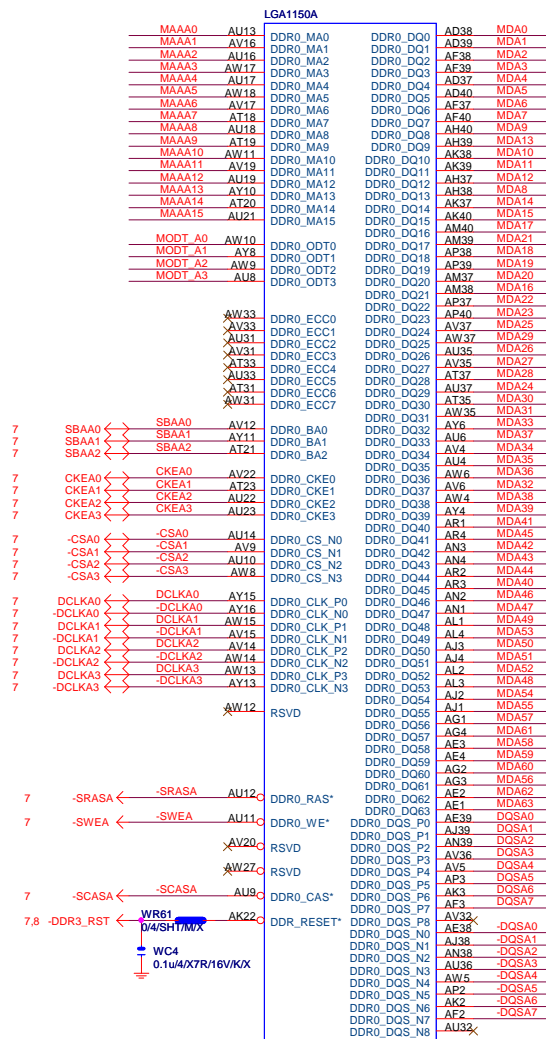
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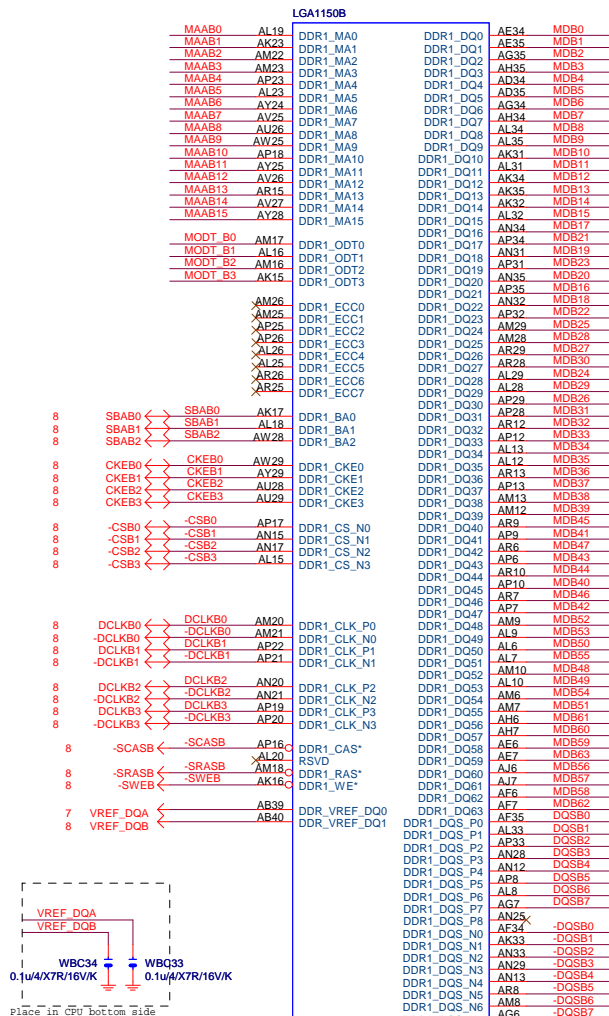
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CPU LGA1150-A			
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(A)



HASWELL/[10SC1-F01150-11R_10SC1-F01150-12R]

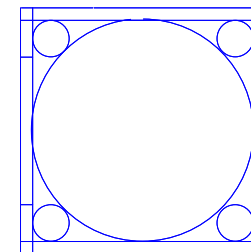
(B)



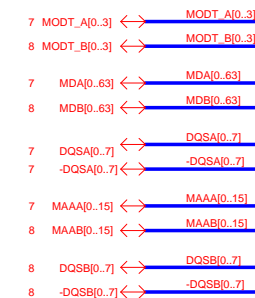
HASWELL/[10SC1-F01150-11R_10SC1-F01150-12R]

(CR)

LGA1150
ILM_BP/1156/CSP/12KRC-0F0001-52R_12KRC-0F0001-51R]



DDR BUS



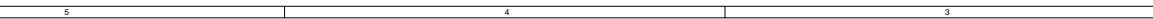
(F, J)



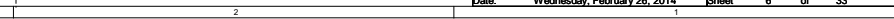
(G,H,I)

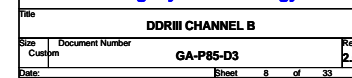


(X30)



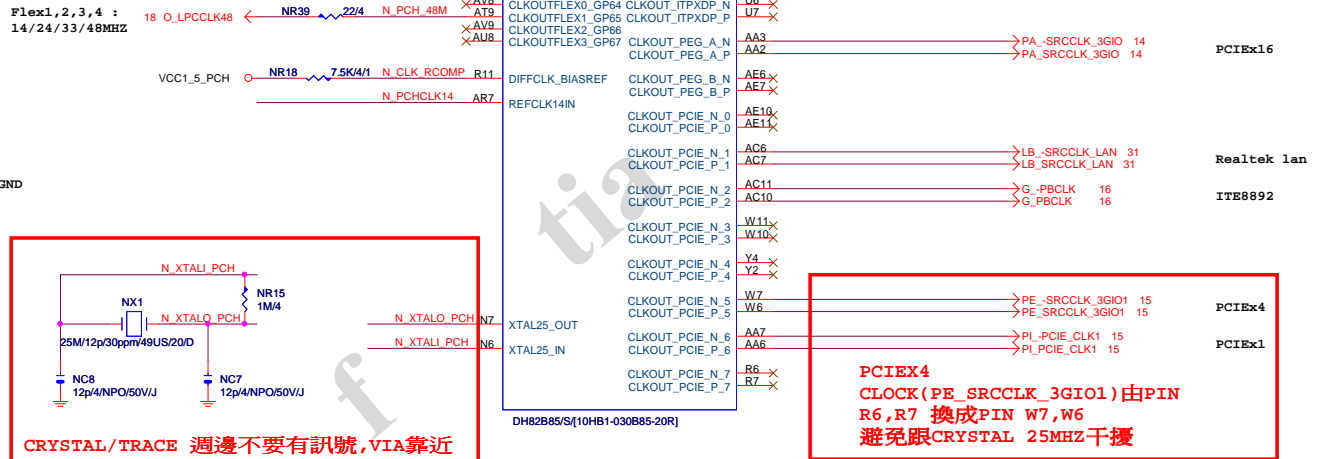
(x15)





[illegible]

Flex1,2,3,4 :
14/24/33/48MHZ



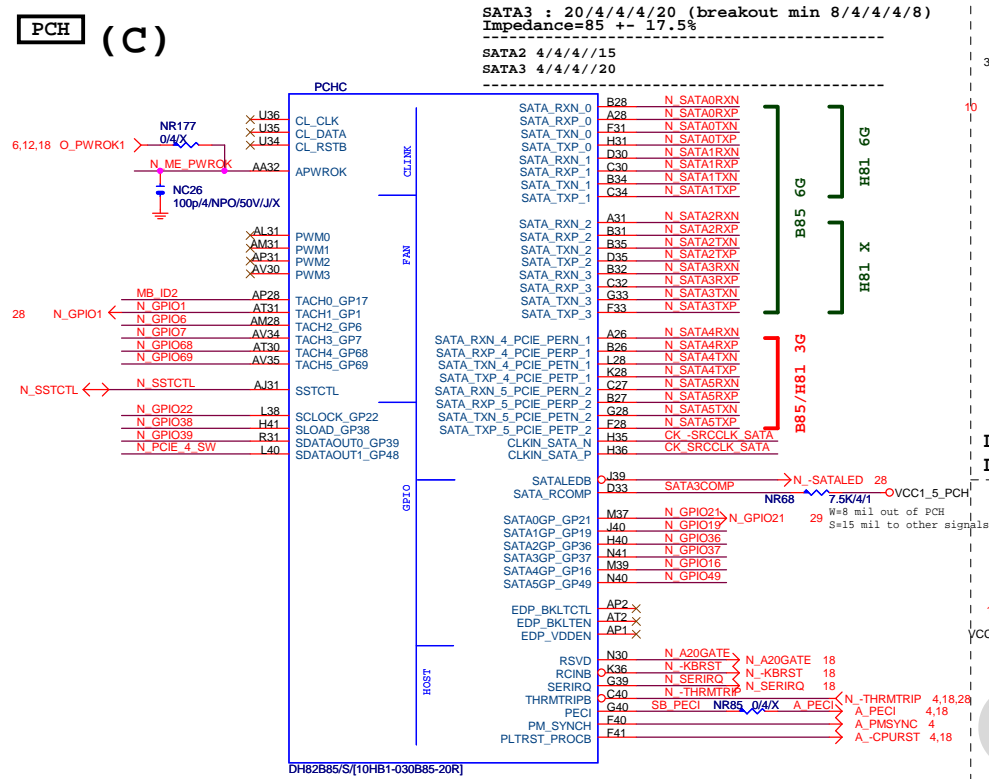
The diagram shows two connection points for the integrated clock generation mode. The first point, labeled 'N_CLK_GND', shows two parallel traces (one red, one blue) connected to a ground symbol. The traces are labeled 'NR42' and 'NR41' respectively, with a value of '8.2K/4' next to each. The second point, labeled 'N_PCHCLK14', shows a single red trace connected to a ground symbol. The trace is labeled 'NR118' with a value of '8.2K/4'.

VGA DDC

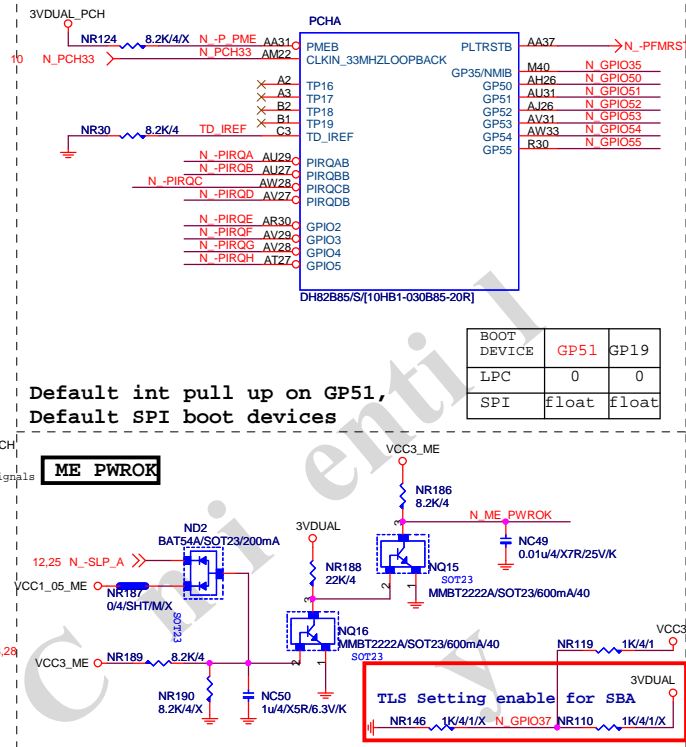
PCIEX4
CLOCK(PE_SRCCLK_3GIO1)由PIN
R6,R7 换成PIN W7,W6
避免跟CRYSTAL 25MHZ干扰

Differential Clock:18/4/6/4/18
Impedance=90 +- 15%

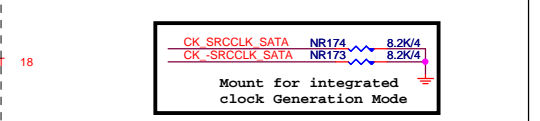
PCH (C)



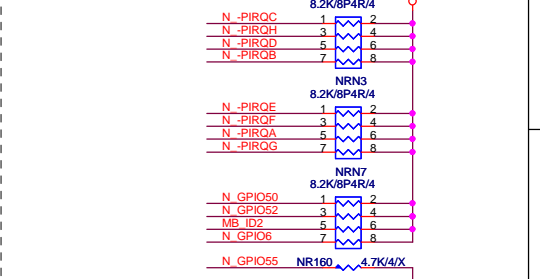
PCH (A)



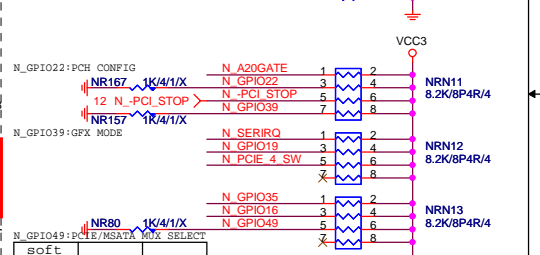
PCH CLK PD



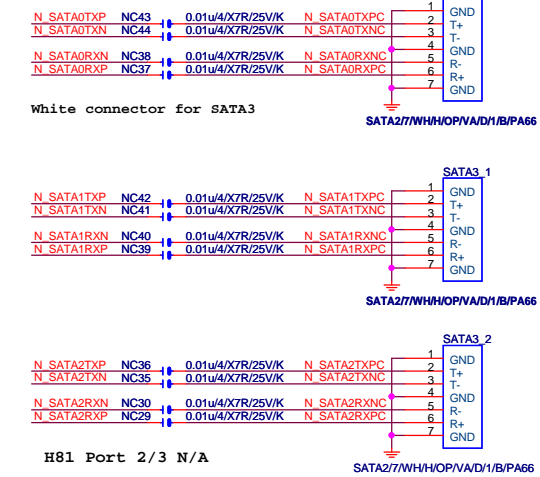
PCH PU/PD



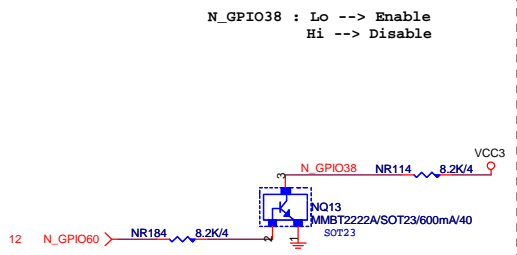
MB ID



SATA CONNECTOR



GPIO38 Ctrl



SATA3.0

Pin	Signal
15	N SATA3TXP
14	N SATA3TXN
13	N SATA3RXN
12	N SATA3RXP
11	N SATA3TXP
10	N SATA3TXN
9	N SATA3RXN
8	N SATA3RXP
7	GND
6	T+
5	T-
4	GND
3	R+
2	R-
1	GND

SATA2.0

Pin	Signal
15	N SATA4TXP
14	N SATA4TXN
13	N SATA4RXN
12	N SATA4RXP
11	N SATA4TXP
10	N SATA4TXN
9	N SATA4RXN
8	N SATA4RXP
7	GND
6	T+
5	T-
4	GND
3	R+
2	R-
1	GND

SATA3.0 to SATA2.0 Adapter

SATA3.0 Pin	SATA2.0 Pin
15	15
14	14
13	13
12	12
11	11
10	10
9	9
8	8
7	7
6	6
5	5
4	4
3	3
2	2
1	1

Notes:

- SATA3.0 (From Z87) - 黑色
- SATA3.0 (From Marvell) - 灰色
- SATA2.0 (From B85) - 黑色
- SATA2.0 (From B85) - 白色

Port 4&5 SATA3.0

Port 4&5 SATA2.0

```
MFG Mode
N_GPIO38 : Lo --> Enable
           Hi --> Disable
```

Gigabyte Technology

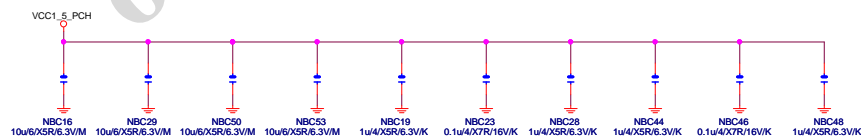
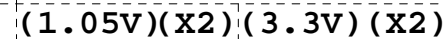
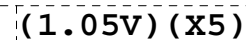
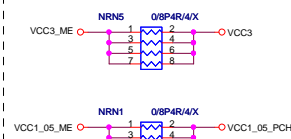
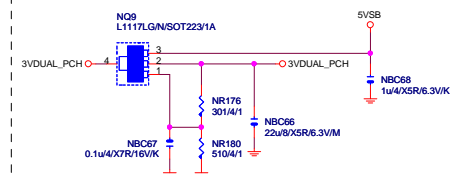
Title			
PCH HOST , SATA, PCI			
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PCH (I)

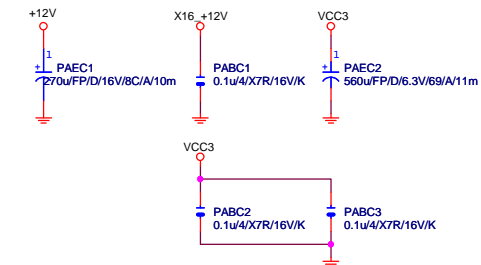


SHT PWR

CAP

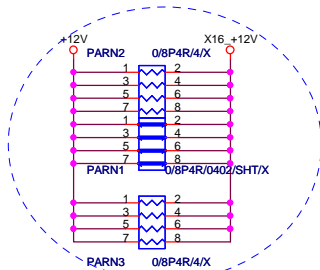


PCIEX16 CAP



PCIEX16 PROTECT SHT

+12 protect
short-wire test



PCIEX16 AC CAP

PA EXP TXP0 C	PAC5	0.22u4/X5R/6.3V/K	PA EXP TXP0 C
PA EXP TXN0 C	PAC4	0.22u4/X5R/6.3V/K	PA EXP TXN0 C
PA EXP TXP1 C	PAC6	0.22u4/X5R/6.3V/K	PA EXP TXP1 C
PA EXP TXN1 C	PAC7	0.22u4/X5R/6.3V/K	PA EXP TXN1 C
PA EXP TXP2 C	PAC8	0.22u4/X5R/6.3V/K	PA EXP TXP2 C
PA EXP TXN2 C	PAC9	0.22u4/X5R/6.3V/K	PA EXP TXN2 C
PA EXP TXP3 C	PAC10	0.22u4/X5R/6.3V/K	PA EXP TXP3 C
PA EXP TXN3 C	PAC11	0.22u4/X5R/6.3V/K	PA EXP TXN3 C
PA EXP TXP4 C	PAC12	0.22u4/X5R/6.3V/K	PA EXP TXP4 C
PA EXP TXN4 C	PAC13	0.22u4/X5R/6.3V/K	PA EXP TXN4 C
PA EXP TXP5 C	PAC14	0.22u4/X5R/6.3V/K	PA EXP TXP5 C
PA EXP TXN5 C	PAC15	0.22u4/X5R/6.3V/K	PA EXP TXN5 C
PA EXP TXP6 C	PAC16	0.22u4/X5R/6.3V/K	PA EXP TXP6 C
PA EXP TXN6 C	PAC17	0.22u4/X5R/6.3V/K	PA EXP TXN6 C
PA EXP TXP7 C	PAC19	0.22u4/X5R/6.3V/K	PA EXP TXP7 C
PA EXP TXN7 C	PAC18	0.22u4/X5R/6.3V/K	PA EXP TXN7 C
PA EXP TXP8 C	PAC20	0.22u4/X5R/6.3V/K	PA EXP TXP8 C
PA EXP TXN8 C	PAC21	0.22u4/X5R/6.3V/K	PA EXP TXN8 C
PA EXP TXP9 C	PAC22	0.22u4/X5R/6.3V/K	PA EXP TXP9 C
PA EXP TXN9 C	PAC23	0.22u4/X5R/6.3V/K	PA EXP TXN9 C
PA EXP TXP10 C	PAC24	0.22u4/X5R/6.3V/K	PA EXP TXP10 C
PA EXP TXN10 C	PAC25	0.22u4/X5R/6.3V/K	PA EXP TXN10 C
PA EXP TXP11 C	PAC26	0.22u4/X5R/6.3V/K	PA EXP TXP11 C
PA EXP TXN11 C	PAC27	0.22u4/X5R/6.3V/K	PA EXP TXN11 C
PA EXP TXP12 C	PAC28	0.22u4/X5R/6.3V/K	PA EXP TXP12 C
PA EXP TXN12 C	PAC29	0.22u4/X5R/6.3V/K	PA EXP TXN12 C
PA EXP TXP13 C	PAC30	0.22u4/X5R/6.3V/K	PA EXP TXP13 C
PA EXP TXN13 C	PAC31	0.22u4/X5R/6.3V/K	PA EXP TXN13 C
PA EXP TXP14 C	PAC32	0.22u4/X5R/6.3V/K	PA EXP TXP14 C
PA EXP TXN14 C	PAC33	0.22u4/X5R/6.3V/K	PA EXP TXN14 C
PA EXP TXP15 C	PAC34	0.22u4/X5R/6.3V/K	PA EXP TXP15 C
PA EXP TXN15 C	PAC35	0.22u4/X5R/6.3V/K	PA EXP TXN15 C

PCI-E REV:1.1--> 2.5GHZ

PCE-E X1(單向) BANDWITH=2.5GHz*(8b/10b)=2Gb/s=250MB/s

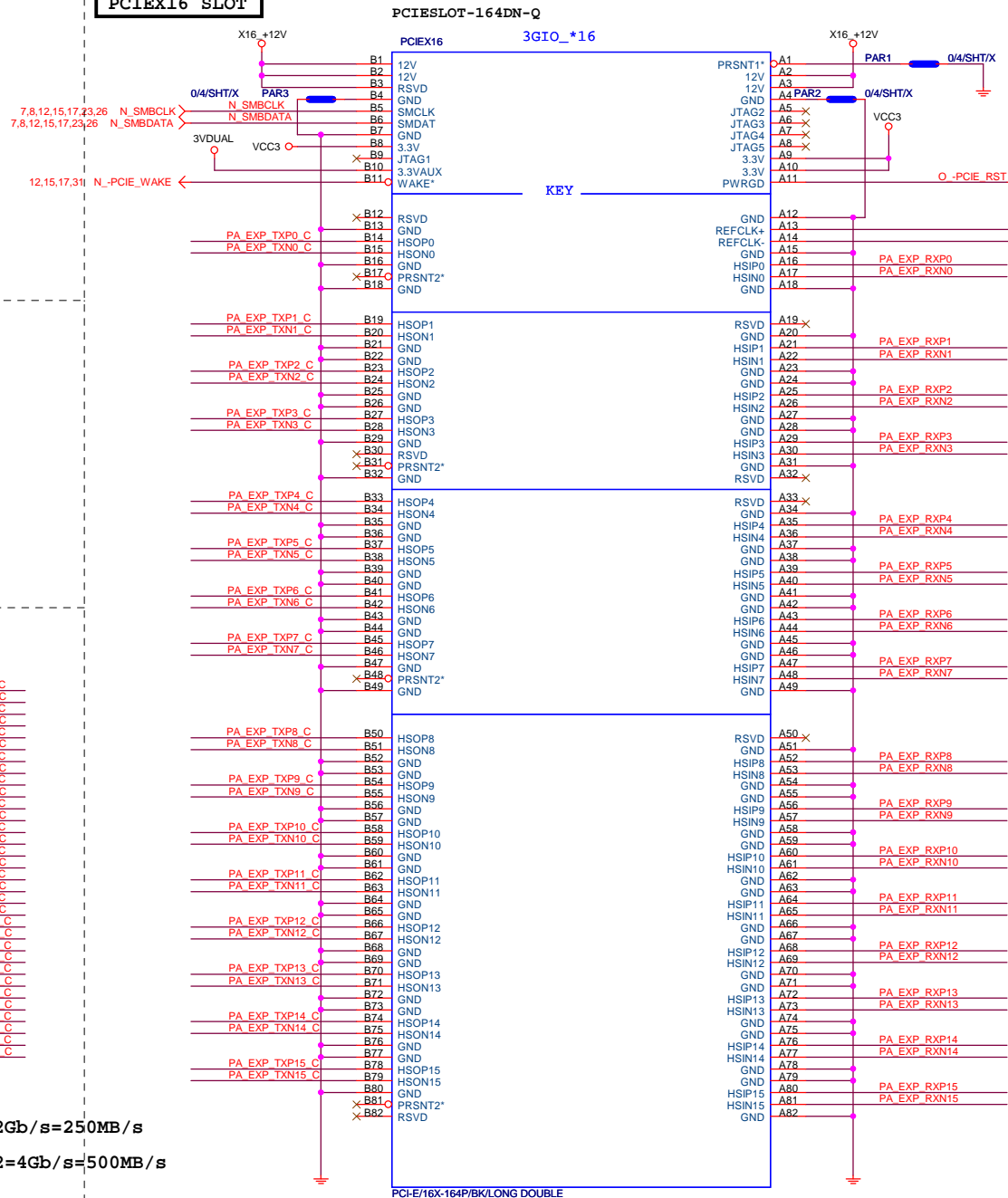
PCE-E X1(雙向) BANDWITH=2.5GHz*(8b/10b)X2=4Gb/s=500MB/s

PCE-E X16(單向) BANDWITH=2.5GHz*(8b/10b)X16=32Gb/s=4GB/s

PCE-E X16(雙向) BANDWITH=2.5GHz*(8b/10b)X16X2=64Gb/s=8GB/s

PCI-E REV:2.0--> 5GHZ

PCIEX16 SLOT

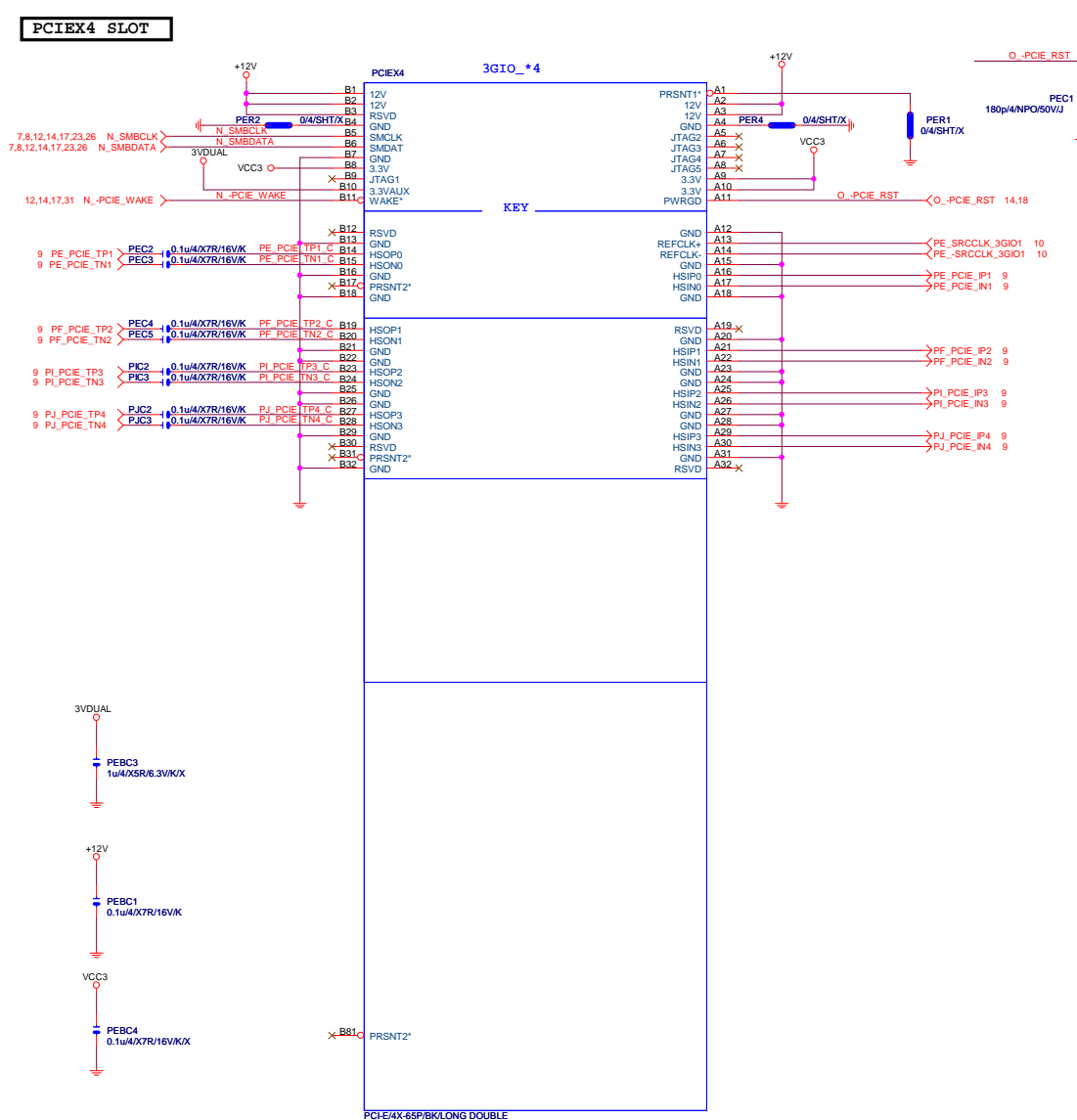


The auxiliary reset circuit is only required for PCIe Gen3 margining and functional link training

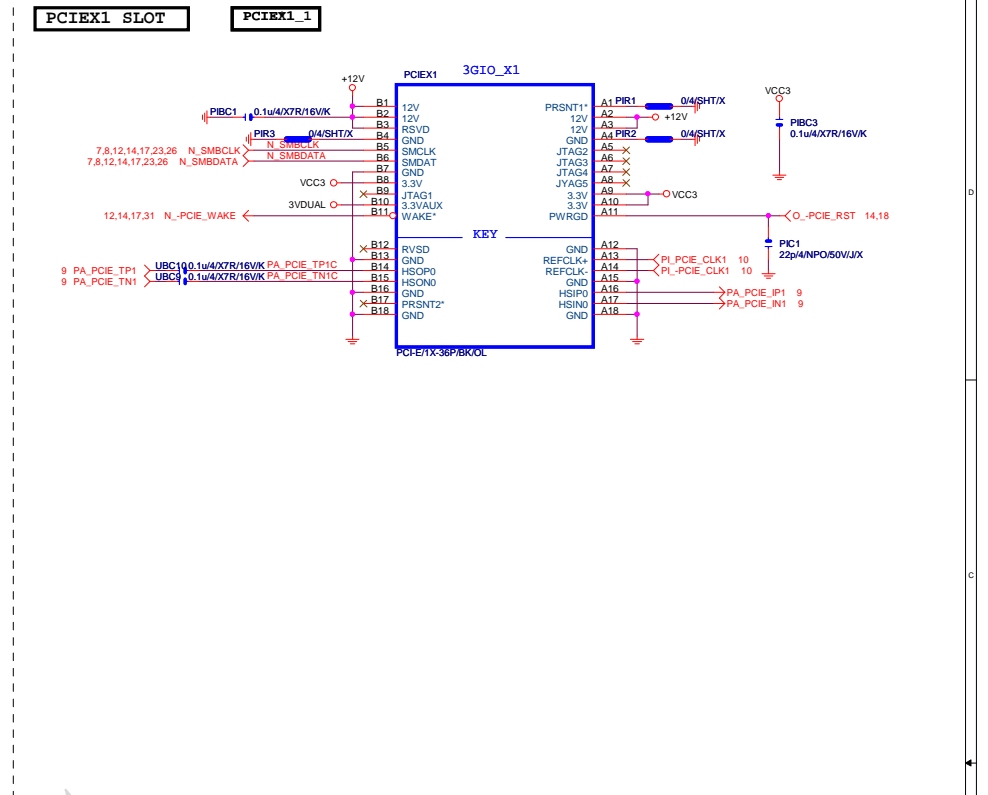
PCIEX16:16/5/5/5/16

PA EXP RXP0[0..15]	>>>PA_EXP_RXP[0..15]	4
PA EXP RXN0[0..15]	>>>PA_EXP_RXN[0..15]	4
PA EXP TXP[0..15]	>>>PA_EXP_TXP[0..15]	4
PA EXP TXN[0..15]	>>>PA_EXP_TXN[0..15]	4

Gigabyte Technology			
PCI EXPRESS * 16			
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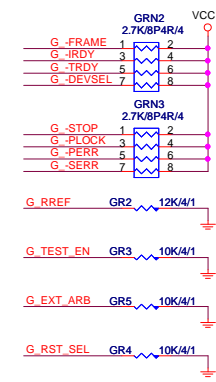
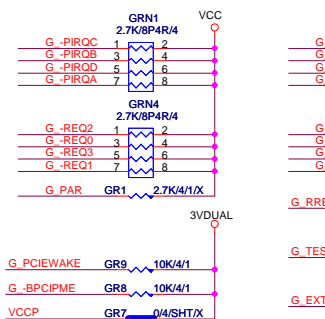
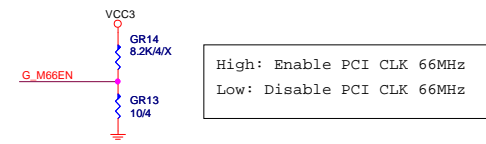
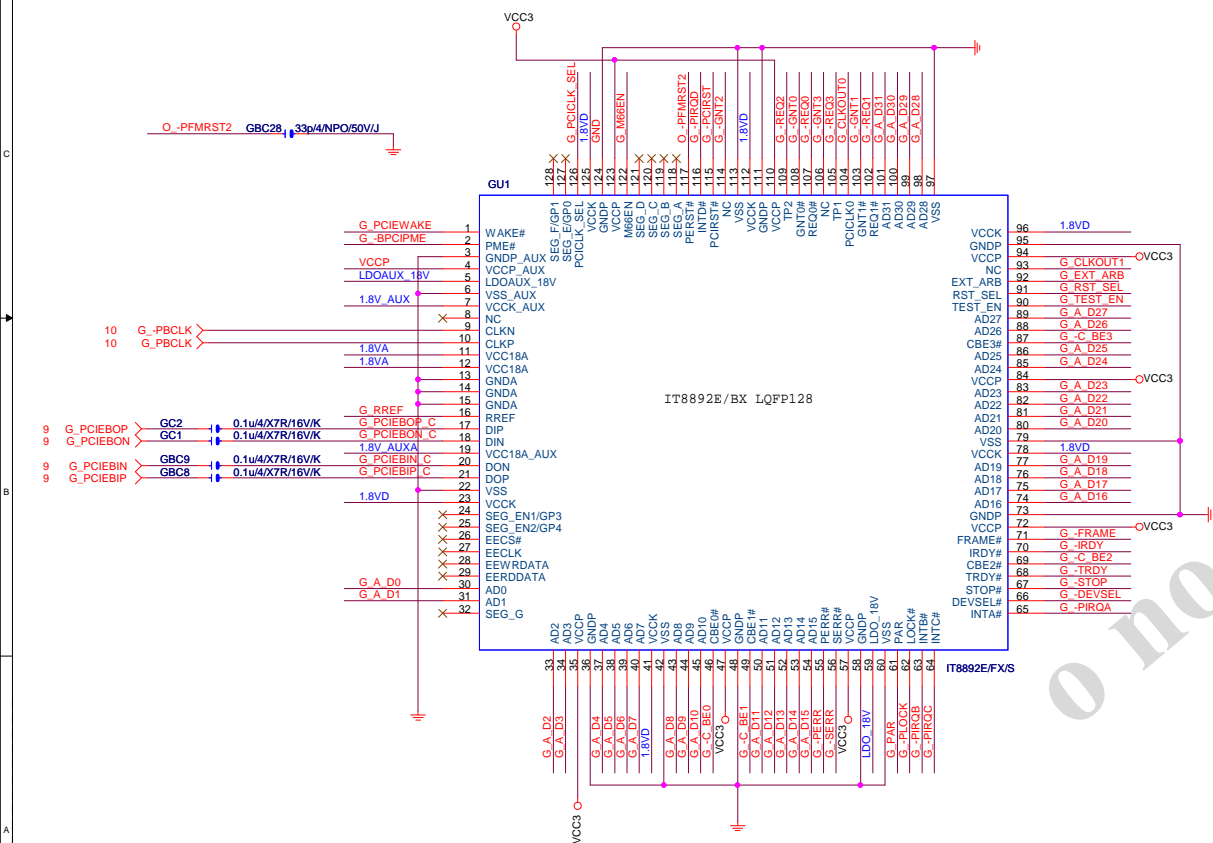
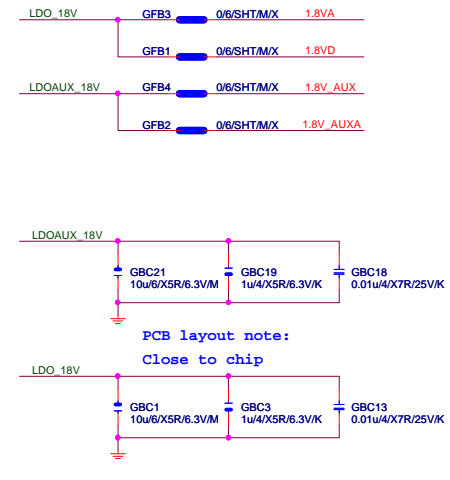
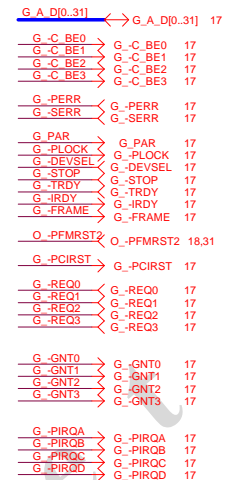



	N_PCIE_4_SW (PCH_GPIO48)	PCIEX4_X1 (SIO_GPIO26)
PCIEX4 No devices	H	H
PCIEX4 -> X1	H	H
PCIEX4 Have devices	L	L
PCIEX4 -> X4	L	L
PCIEX1_1/2 --> N/A		

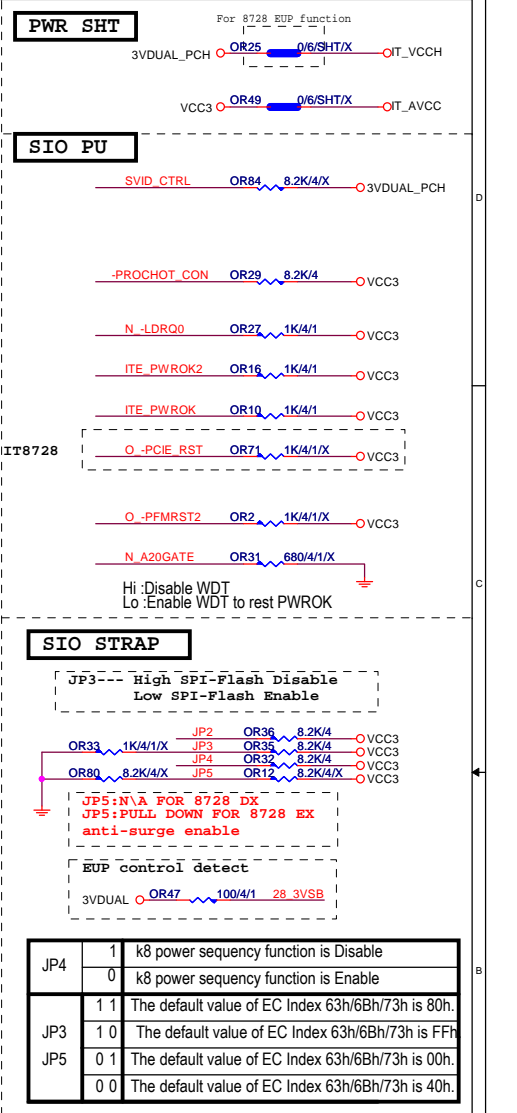
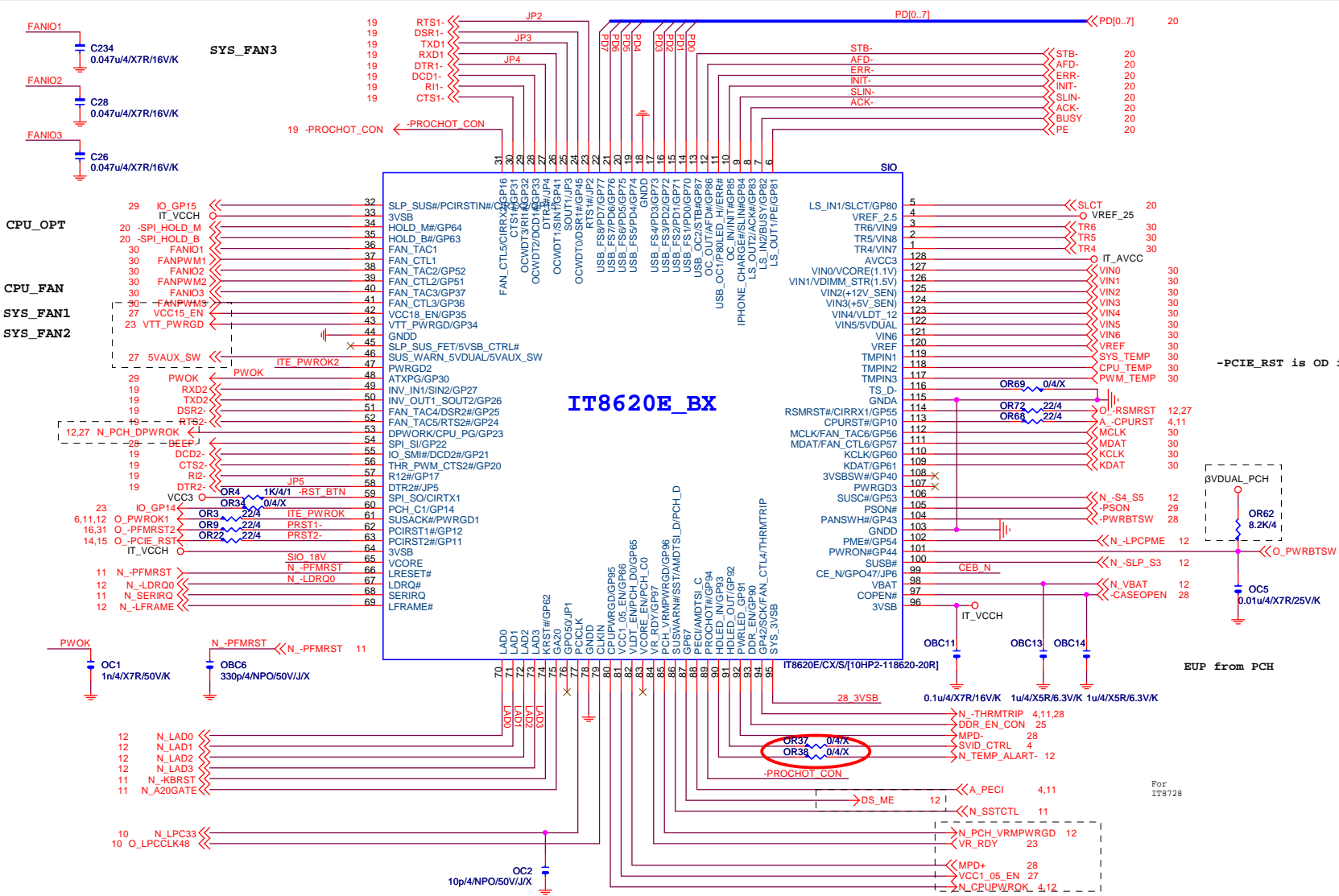


PCIEX4/X1 SWITCH

Function	SEL
xI--> x0a	L;PCIEX4 SLOT-->X1
xI--> x0b	H;PCIEX4 SLOT-->X4

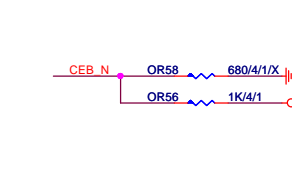


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IT8892E				
Size Custom	Document Number			Rev
	GA-P85-D3			2.0
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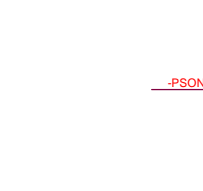


IT8620E GPIO問題匯整	
PIN 50	GP26--- 第一次接上POWER時會拉 LO
PIN 90/91	DEFAULT為HDLED FUNCTION, GP93 BYPASS TO GP92
PIN 108	GP40--- POWER ON 時會拉 LO
PIN 111/112	MOUSE 跟FAN6 FUNCTION 擇一使用, 不然會互相干擾

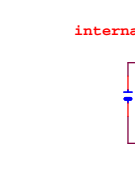
DUAL BIOS OPT STRAP



Power leakage



SIO_18V

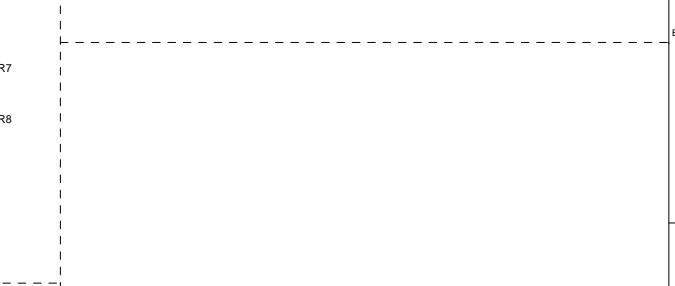
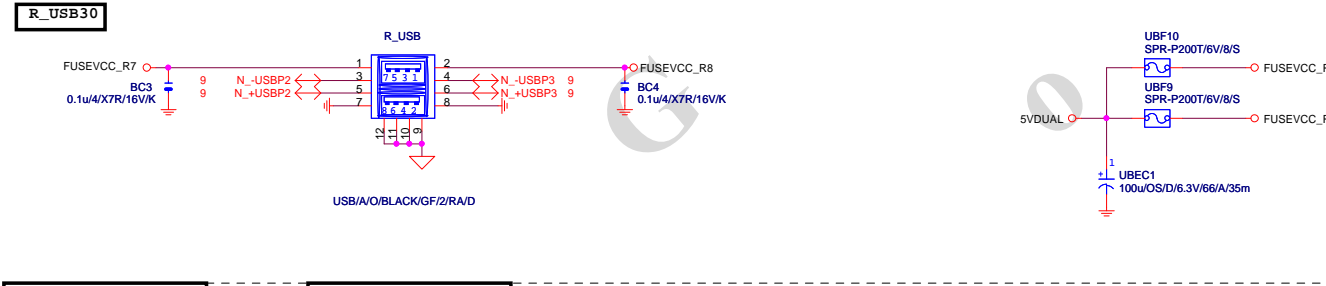
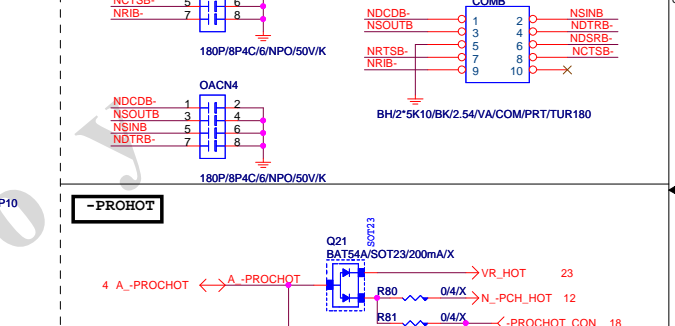
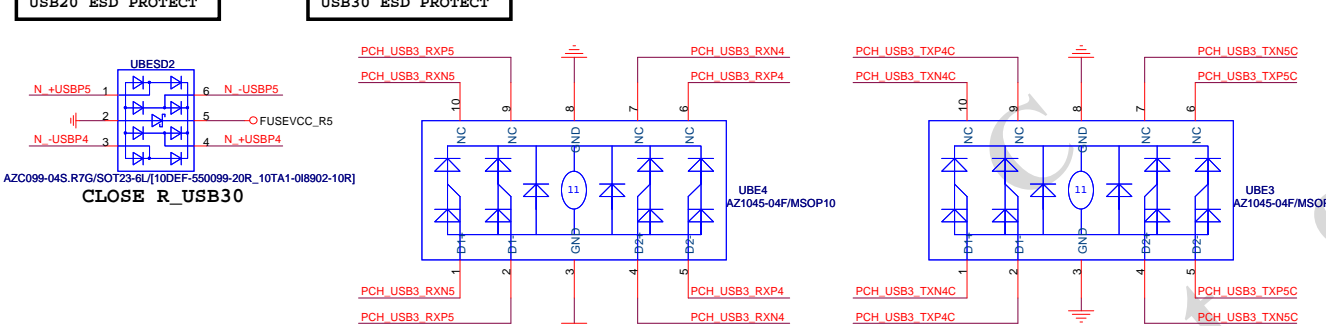
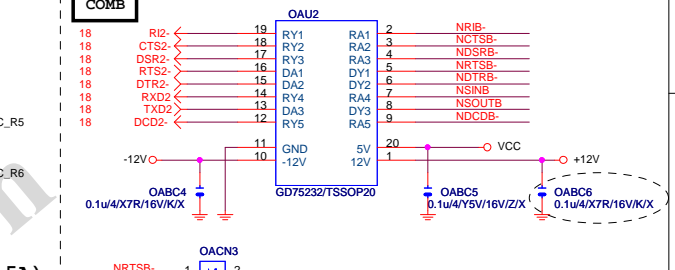
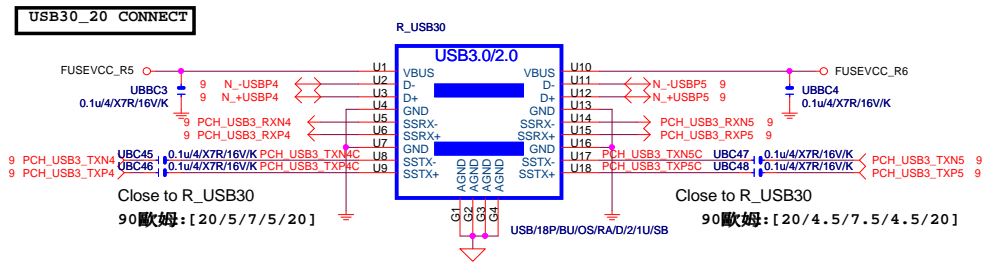
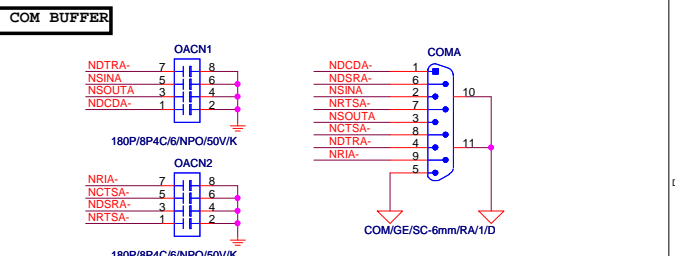
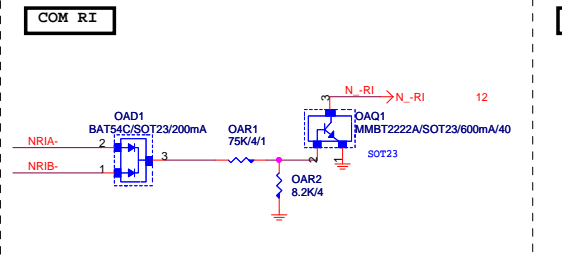
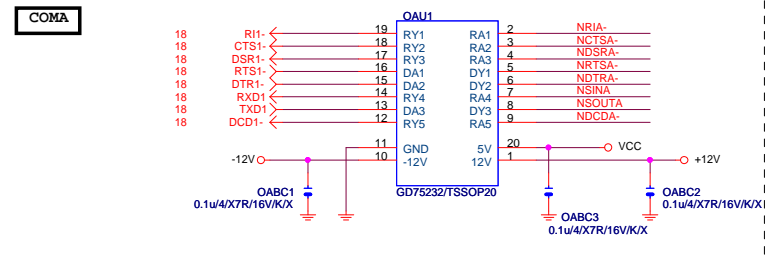


SIO CAP

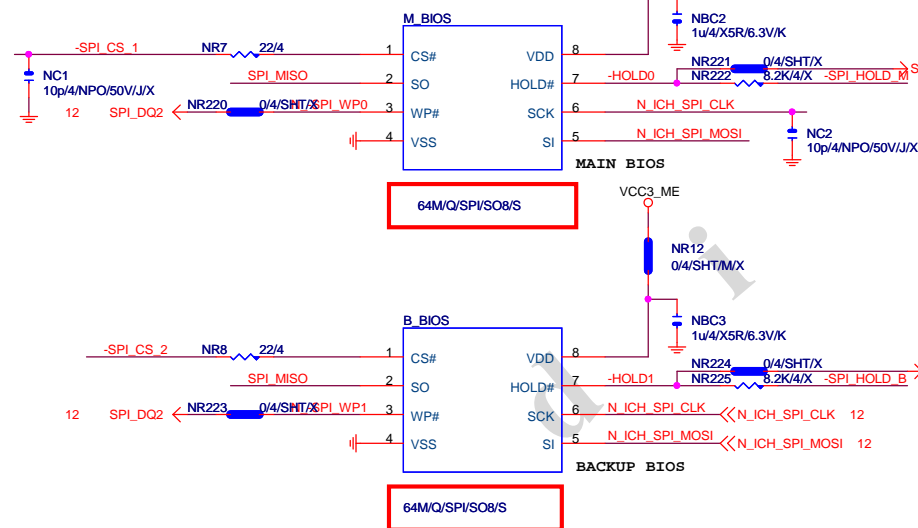
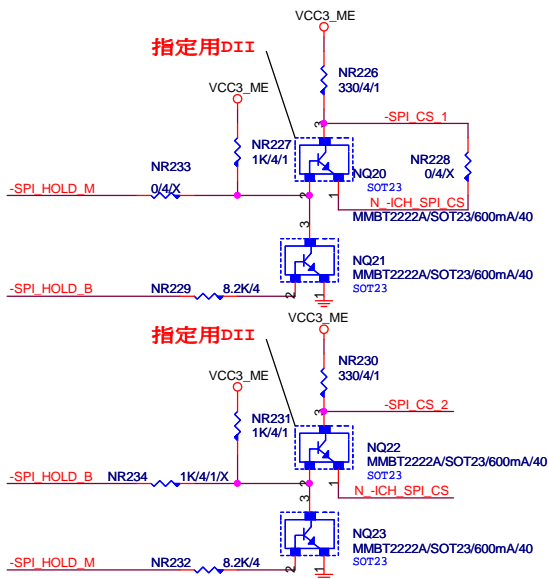


Gigabyte Technology

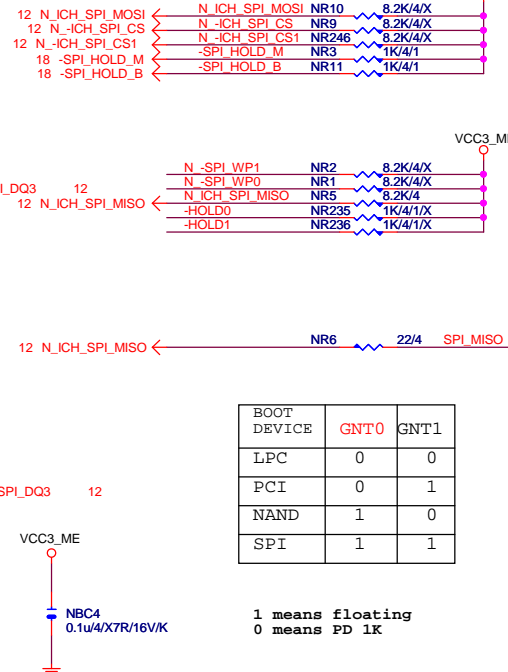
Title		ITE 8620 LPC IO	
Size B	Document Number	GA-P85-D3	
Date:	Wednesday, February 26, 2014	Sheet	18 of 33



DUAL BIOS



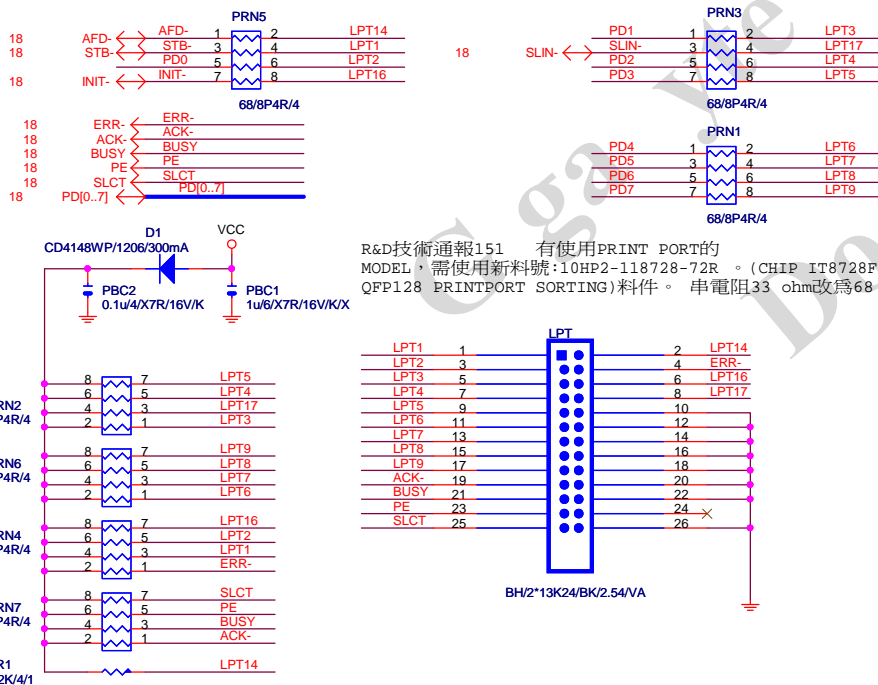
MOSI For DMI RX Termination Voltage



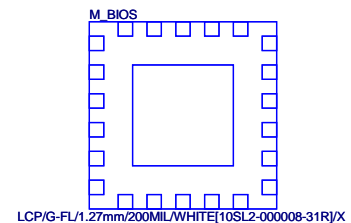
BOOT DEVICE	GNT0	GNT1
LPC	0	0
PCI	0	1
NAND	1	0
SPI	1	1

```
1 means floating
0 means PD 1K
```

LPT PORT



R&D技術通報151 有使用PRINT PORT的
MODEL，需使用新料號：10HP2-118728-72R。(CHIP IT8728F/EX (GB) ITE/SMD
QFP128 PRINTPORT SORTING)料件。串電阻33 ohm改為68 ohm。



M_BIOS

LCP/G-FL/1.27mm/200MIL/WHITE[10SL2-000008-31R]/X

Gigabyte Technology

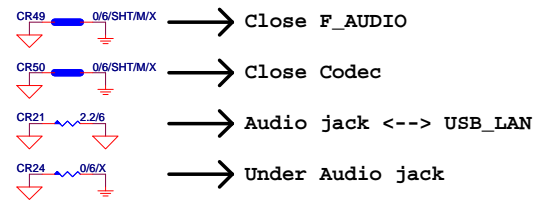
Title		BIOS	
Size Custom	Document Number	GA-P85-D3	Rev 2.0
Date:	Wednesday, February 26, 2014	Sheet 20 of 33	

FOR ON/OFF PLAY

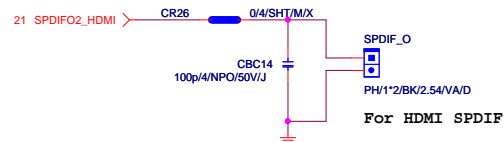


Size	Document Number	GA-P85-D3
Custom		

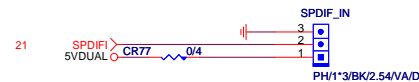
Date: Wednesday, February 26, 2014 Sheet 21 of 33



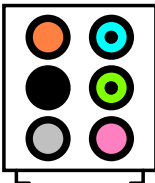
SPDIF_OUT



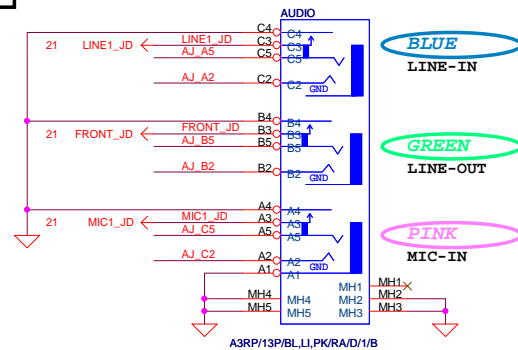
SPDIF_IN



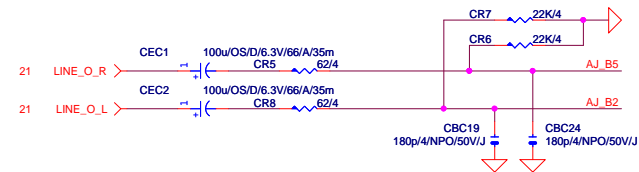
AZALIA JACK



AZALIA JACK



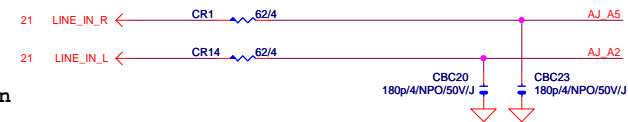
LINE-OUT



LINE-IN

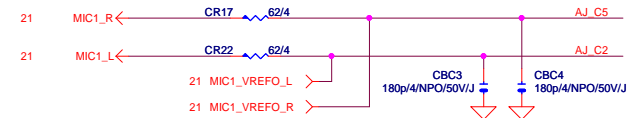
Verify MIC function in LINE-in

Only reserved for ALC888



For 889A/888

MIC-IN

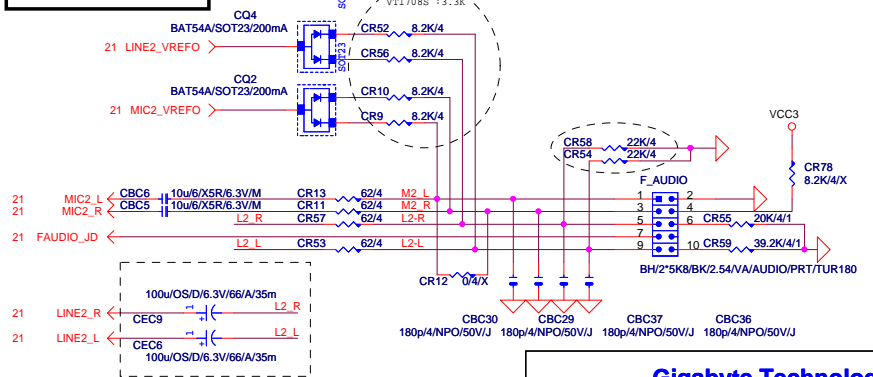


SURROUND

CEN/LFE

SURR BACK

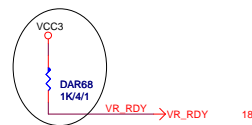
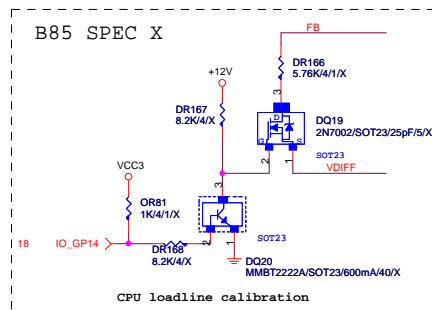
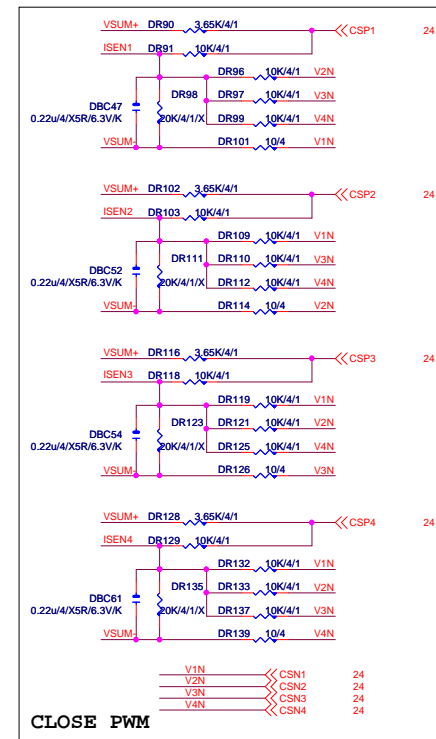
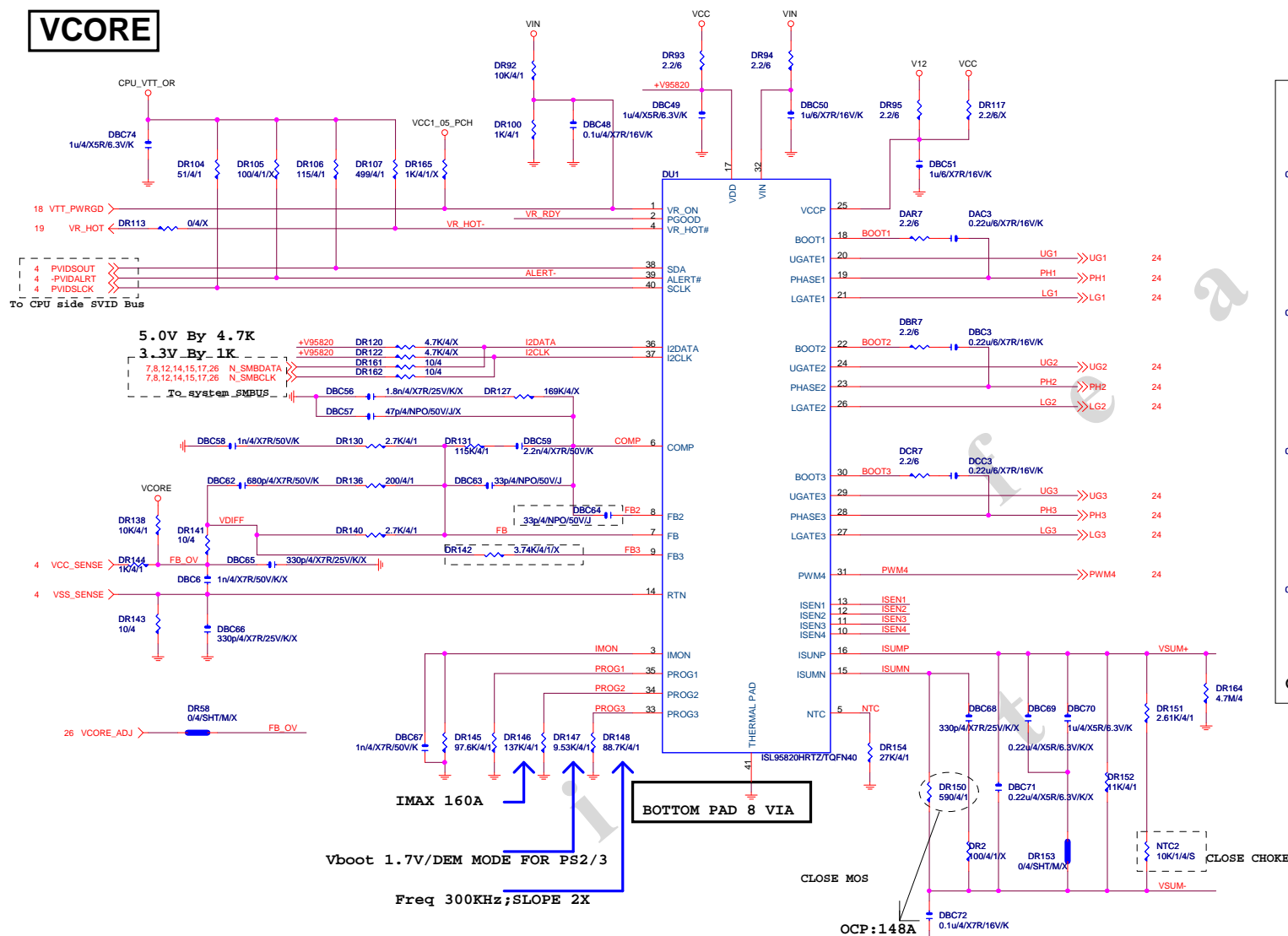
AZALIA FRONT PANEL



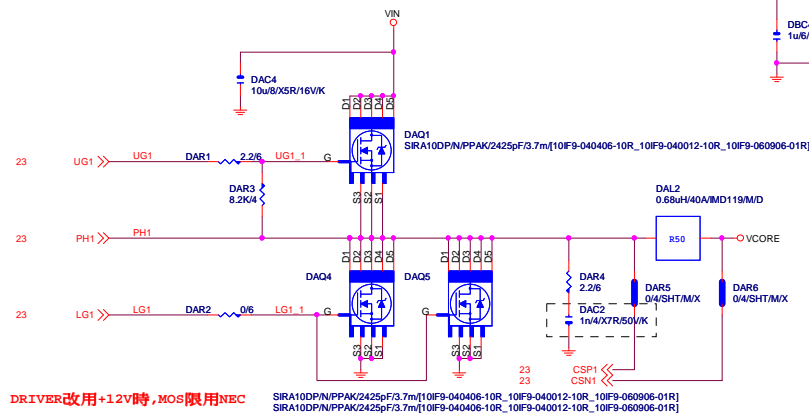
Gigabyte Technology

AUDIO JACK

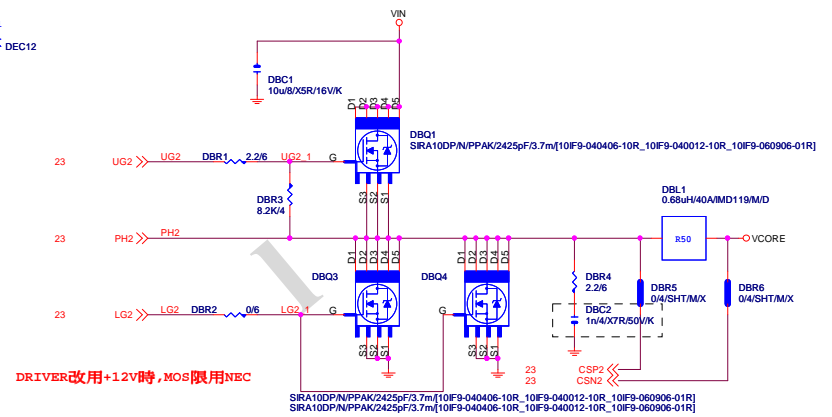
Title	Document Number	Rev
	GA-P85-D3	2.0
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VCORE

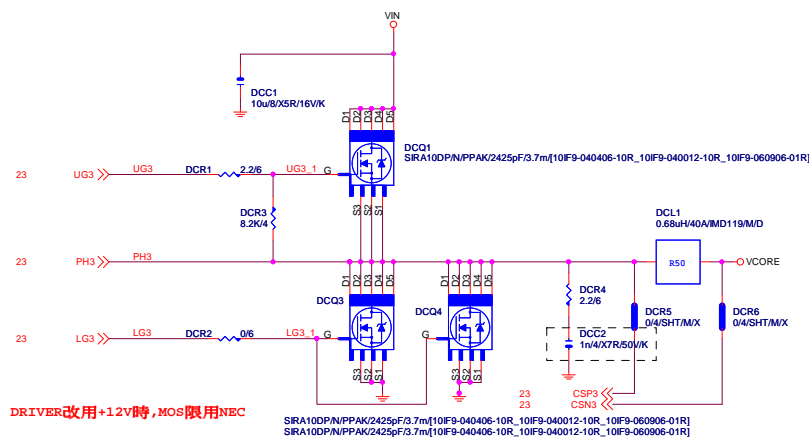
[1]



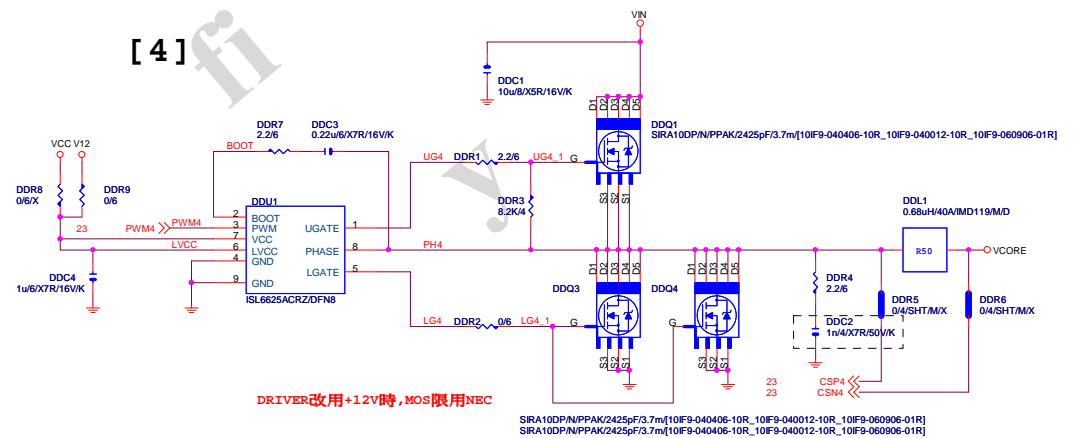
[2]



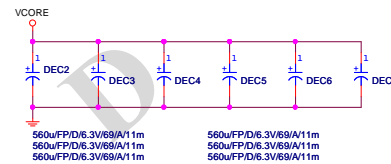
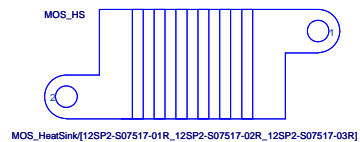
[3]



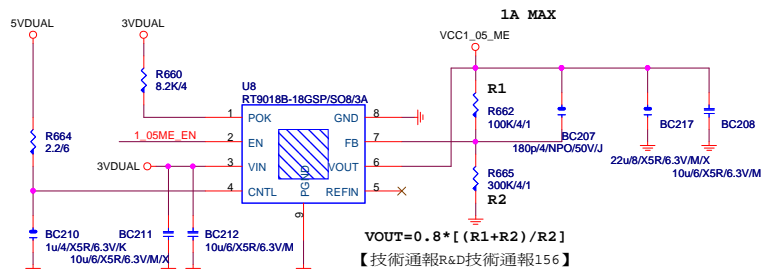
[4]



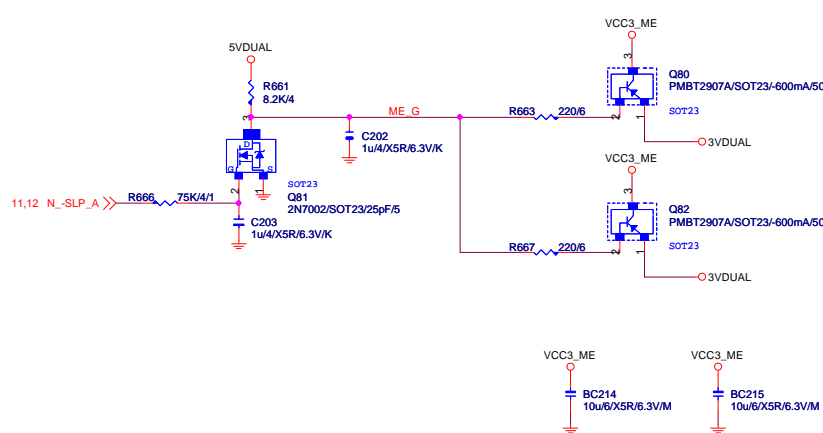
MOSFET HEATSINK



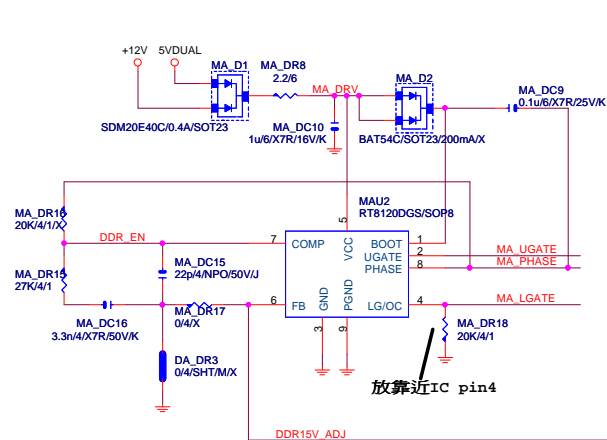
VCC1_05_ME



VCC3_ME

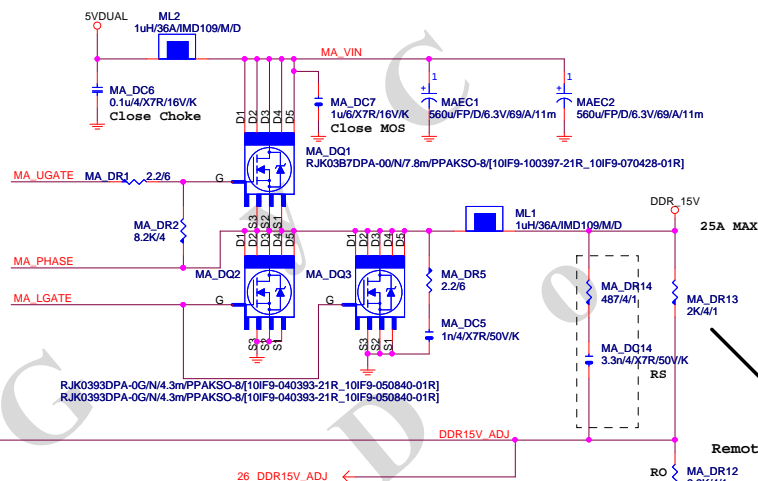


DDR_15V



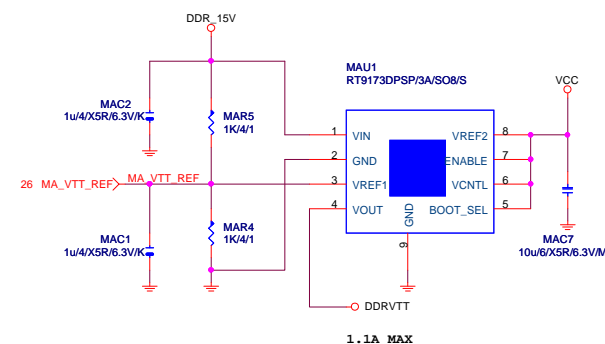
DDR15V_ADJ

PWR SEQ



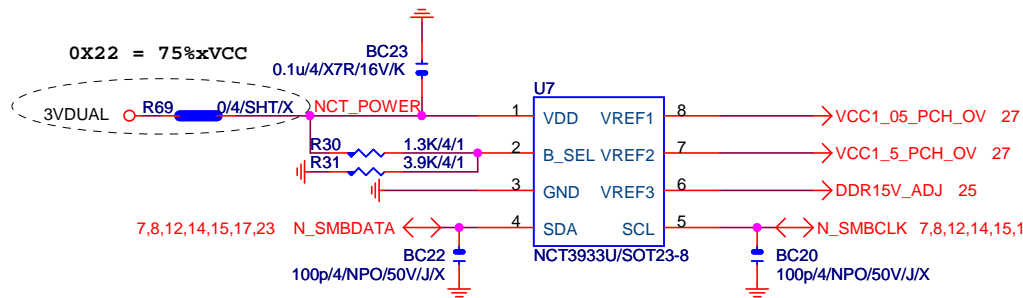
VIN=5V,VOUT=1.5V,IOUT=25A,PHASE=1
IRMS=11.45A
560u/FP/D/6.3V/68/8m RIPPLE CURRENT=4.7A
Coefficient=1.7(85°C),1(105°C)
VIN Ripple current=4.7X1.7=7.99A(85°C)
-->故固態電容須2X7.99=15.98>11.45A
OCP:35.82A for Rds=6.7m for vishay@4.5V
OCP:72.727A for Rds=3.3m for renesas@10V
OCP:48A=Roset*Iocset / Rds(on)
=12K*10uA / [5//5]

DDRVTT

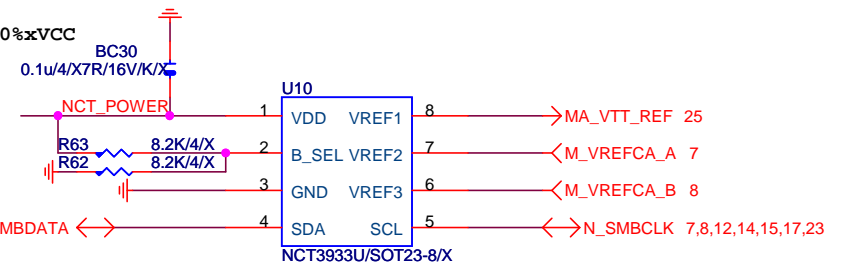


GIGABYTE™			
Title			
DDR15V / M3 POWER			
Size	Document Number	Rev	
Custom	GA-P85-D3	2.0	
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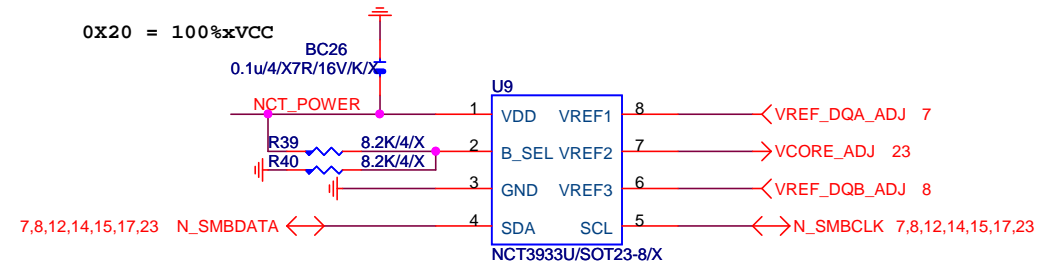
OVER VOLTAGE



0X2A = 0%xVCC



0X20 = 100%xVCC

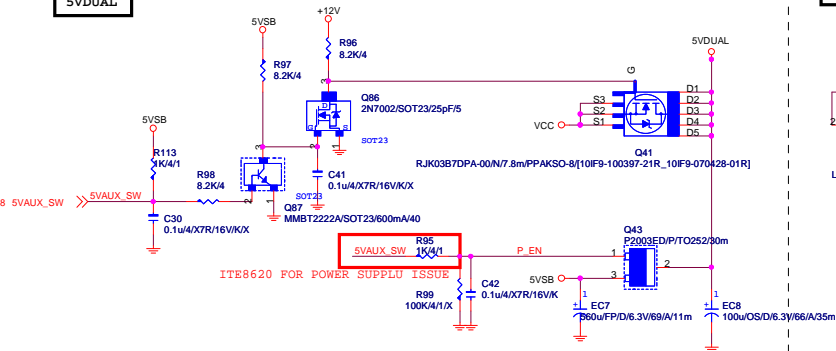


NCT3933	0X2A	0X20	0X22
VREF1	DDRVTT	VREF_DDRA_DQ	PCH Core
VREF2	VREF_DDRA_CA	N/A	VCC1_5_PCH
VREF3	VREF_DDRA_CA	VREF_DDRB_DQ	SMREF

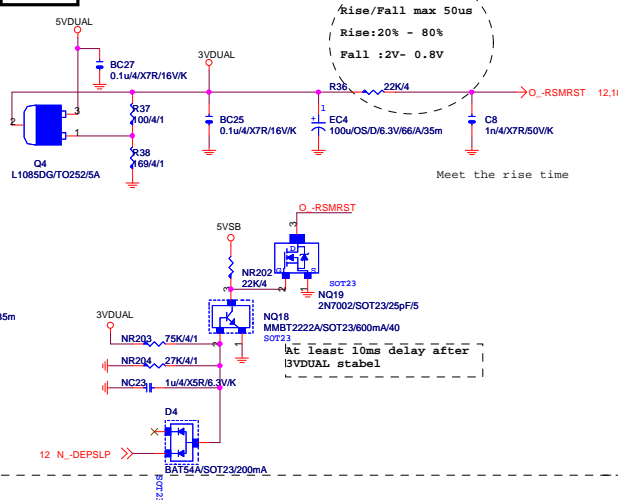
Gigabyte Technology

Title		
CPU CORE VR-2		
Size	Document Number	Rev
Custom	GA-P85-D3	2.0
Date:	Wednesday, February 26, 2014	Sheet 26 of 33

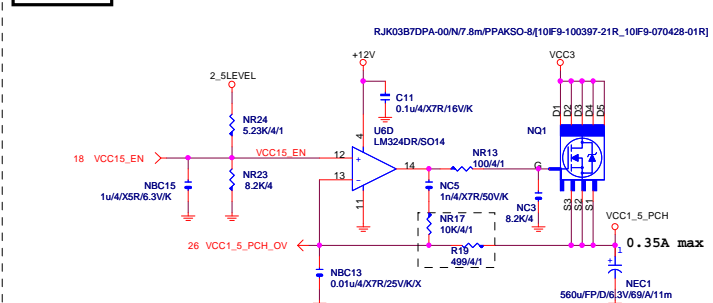
5VDUAL



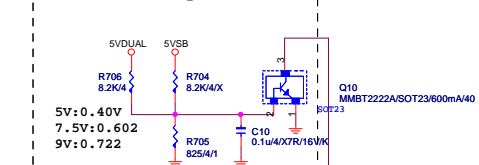
3VDUAL



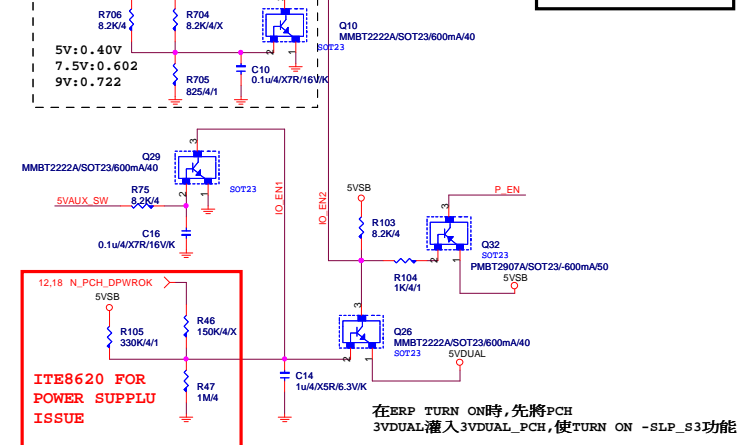
VCC1_5_PCH



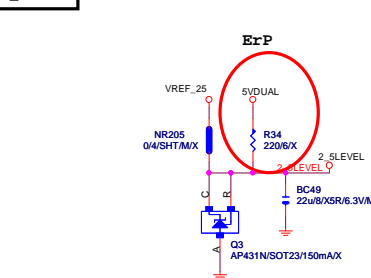
5VSB OVP:7.5V protection



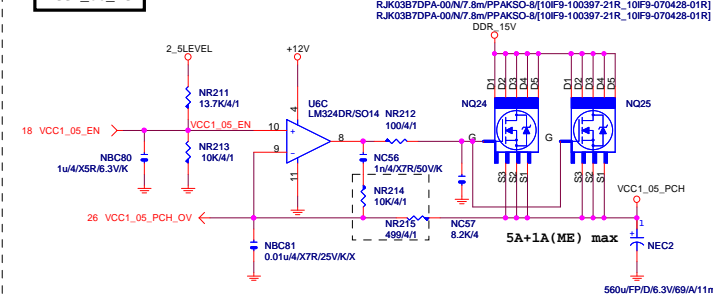
5VDUAL SHORT PROTECT



2_5LEVEL



VCC1_05_PCH



PWR_SEQ

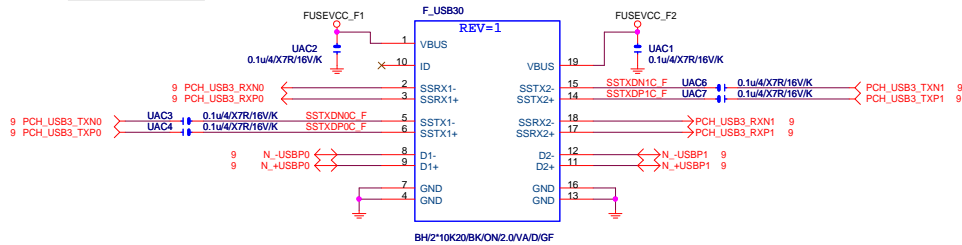
PCH ERP



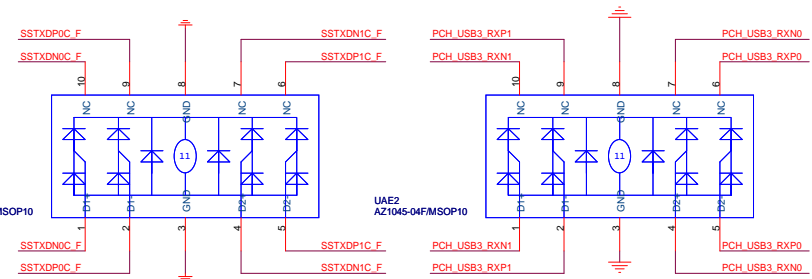
Gigabyte Technology

Title			
DISCRETE POWER			
Size	Document Number	Rev	
Custom	GA-P85-D3	2.0	
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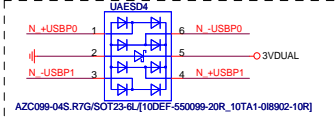
Front USB3.0



F_USB30 ESD PROTECT

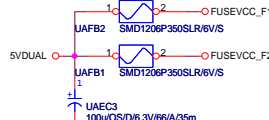


BLUE

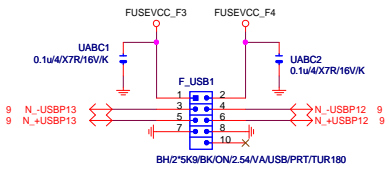


Close to connector

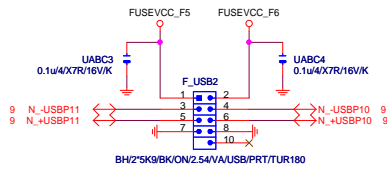
F_USB30 PWR



FRONT USB1



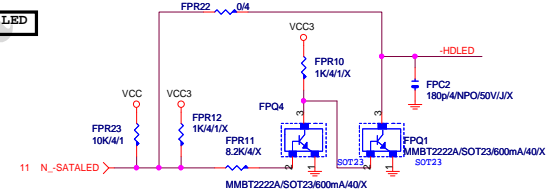
FRONT USB2



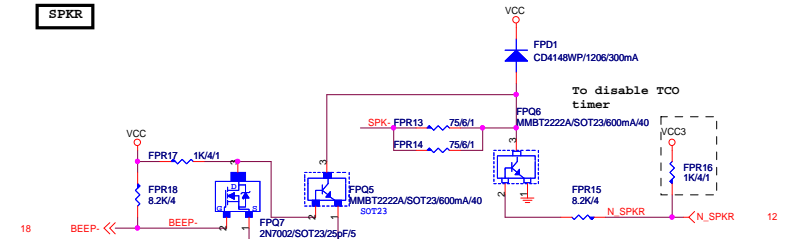
FRONT USB3



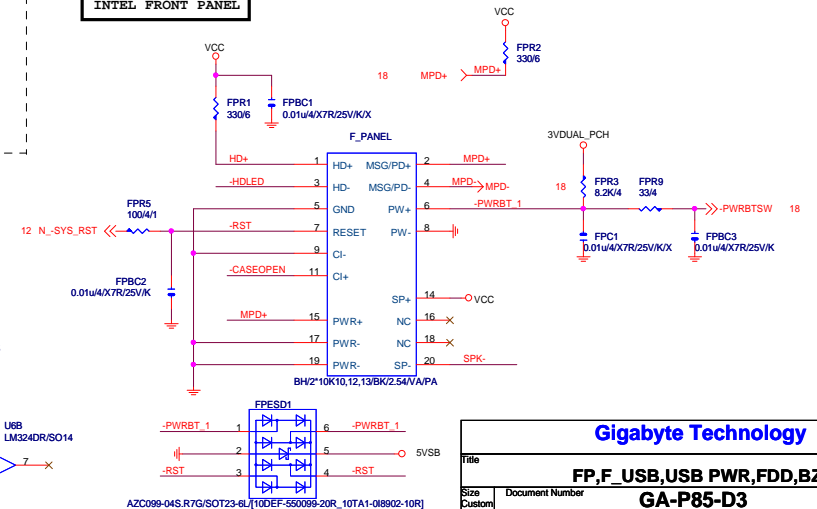
SATA LED



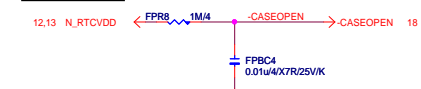
SPKR



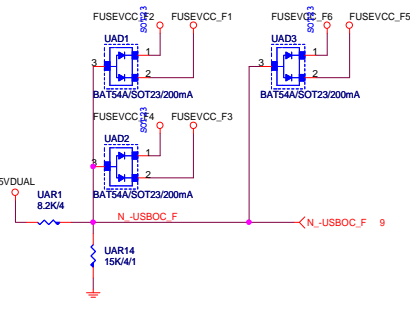
INTEL FRONT PANEL



CASE OPEN



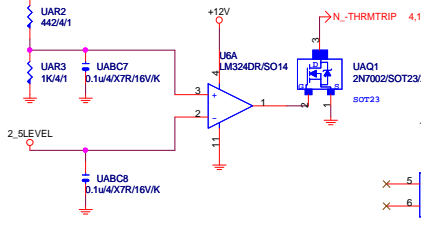
-USBOC_F



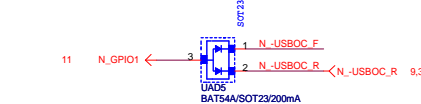
USB2.0 Signal & power short protection

USB2.0 Signal > 4.85V

Enable --> 3VUUAL=3.75V



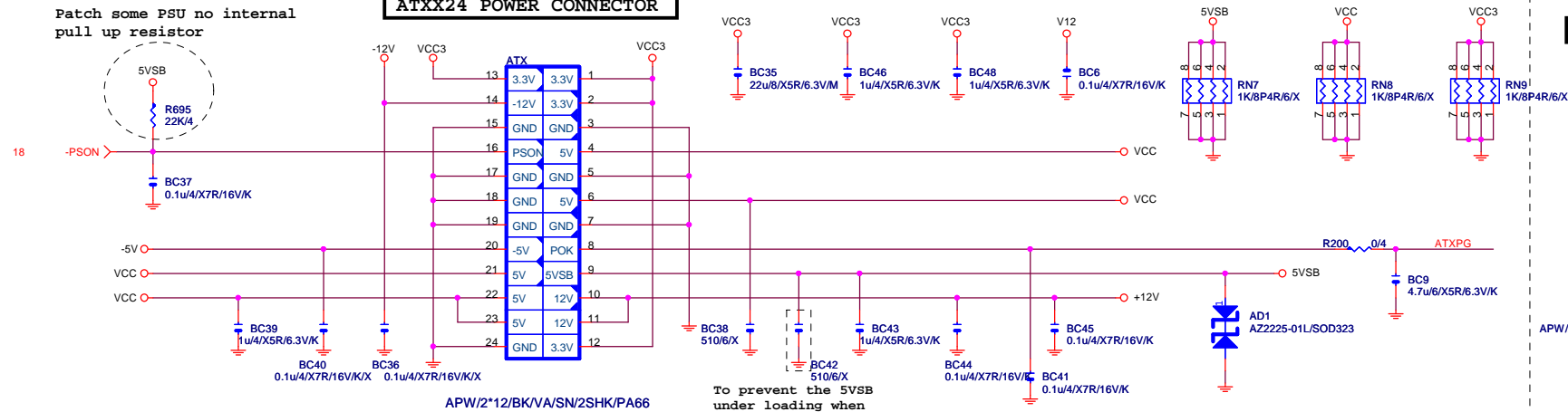
F_USB POWER PROTECT



Gigabyte Technology			
FP,F_USB,USB PWR,FDD,BZ			
GA-P85-D3			
Rev	2.0		
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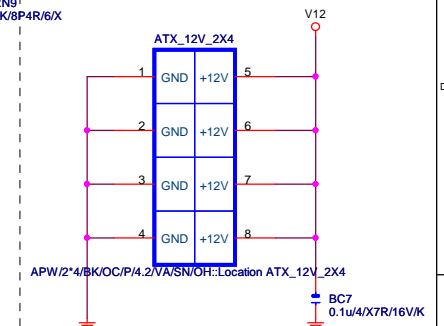
Patch some PSU no internal pull up resistor

ATXX24 POWER CONNECTOR

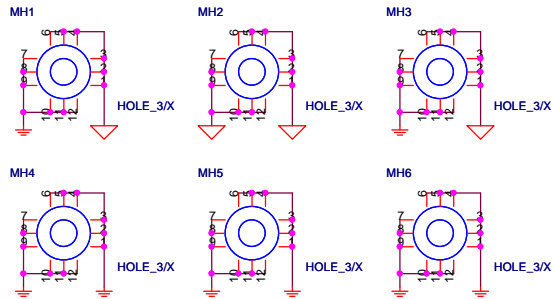


APW/2*12/BK/VA/SN/2SHK/PA66

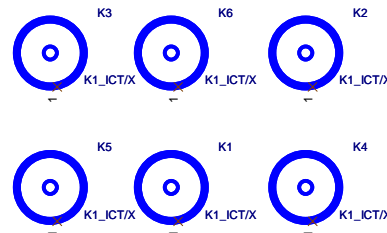
ATXX4 POWER CONNECTOR



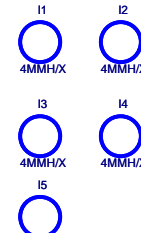
APW/2*4/BK/OC/P/4.2/VA/SN/OH:Location ATX_12V_2X4



HOLE_4-RH-1



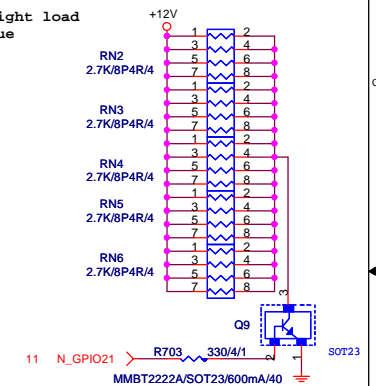
K1-1CT



4MMH

【技術通報R&D技術通報153】

To fix 12V light load abnormal issue



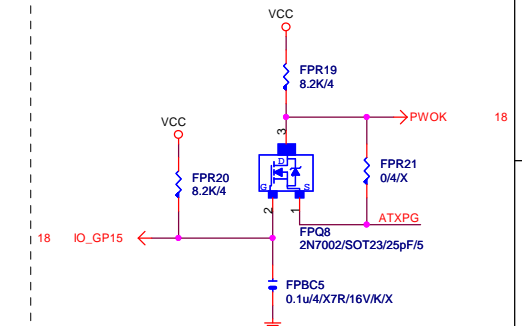
CLK GEN

CPU Frequency Selection

FSLB	FSLA	CPU
0	0	100M <Default>
0	1	133M
1	0	200M
1	1	166M

PWOK PATCH

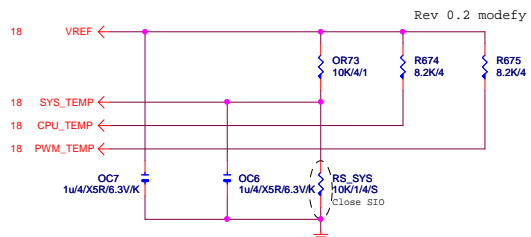
【技術通報R&D技術通報154】



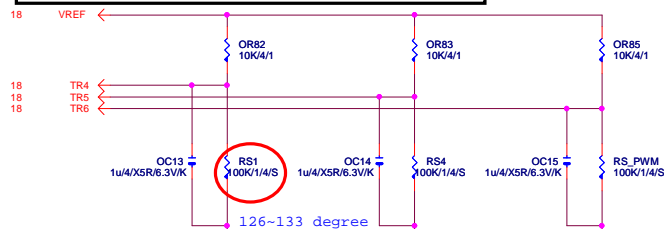
Gigabyte Technology

Title		
ATX POWER CONNECTOR		
Size	Document Number	Rev
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TEMP H/W MONITOR

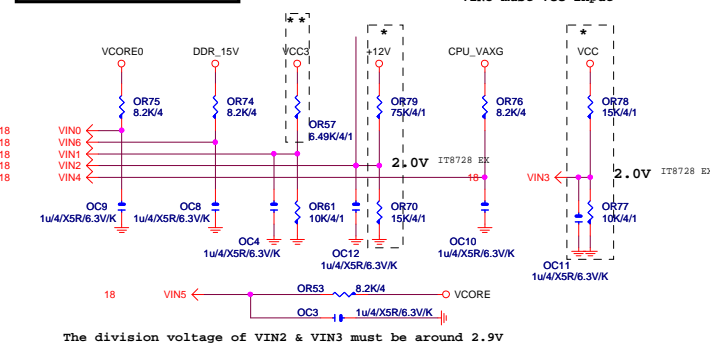


-PROCHOT:有mos heatsink不用prochot function

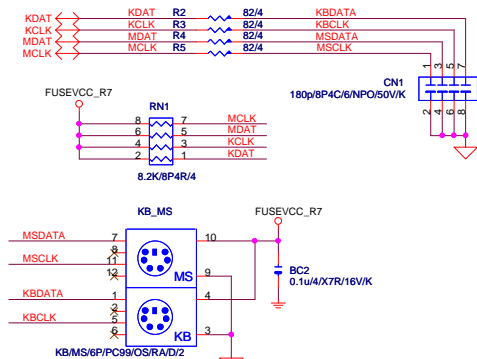


RS1、RS2、RS3 CLOSE CPU VR MOSFET

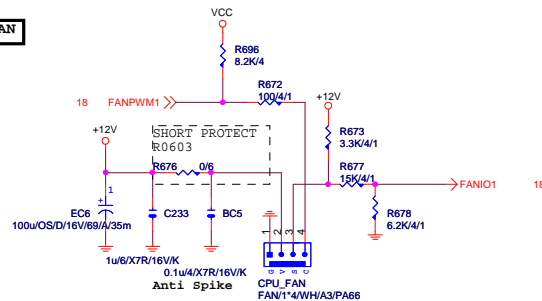
VOLTAGE-- H/W MONITOR



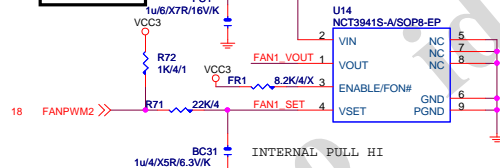
KB/USB



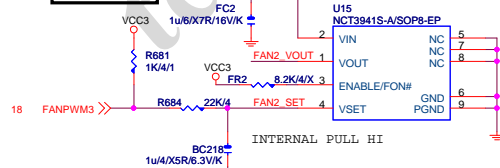
CPU SMART FAN



SYS_FAN_1

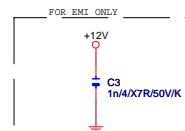
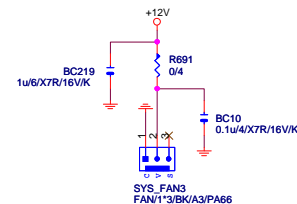


SYS_FAN_2



SYS_FAN_3

Linear SYS_FAN

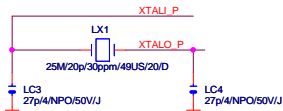


Gigabyte Technology

Title		HWM,KB/MS, FAN CTRL	
Size	Document Number	GA-P85-D3	
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LAN:INTEL I217

100歐姆:[20/4/8/4/20]

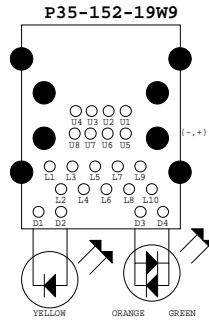
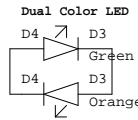
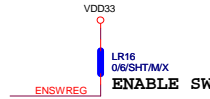


80歐姆:[15/5/5/5/15]

SRCLK 50歐姆:[18/4/10/4/18]

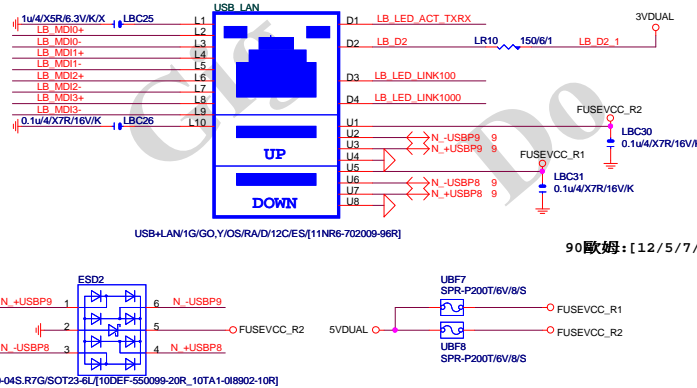
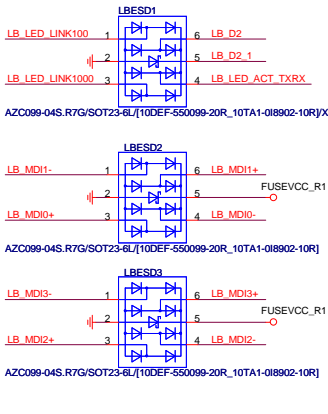
離IC越近越好

FOR DSM MODE
(DEEP SLEEP MODE)

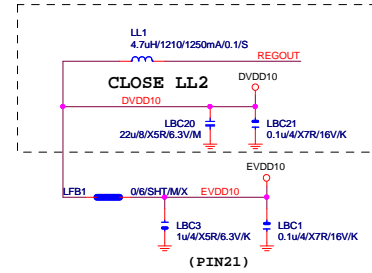
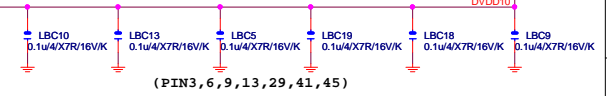
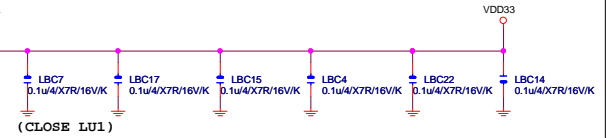


USB30_LAN CONNECTOR

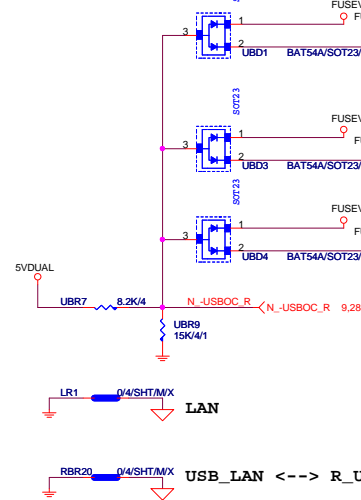
100歐姆:[20/4/8/4/20]



90歐姆:[12/5/7/5/12]



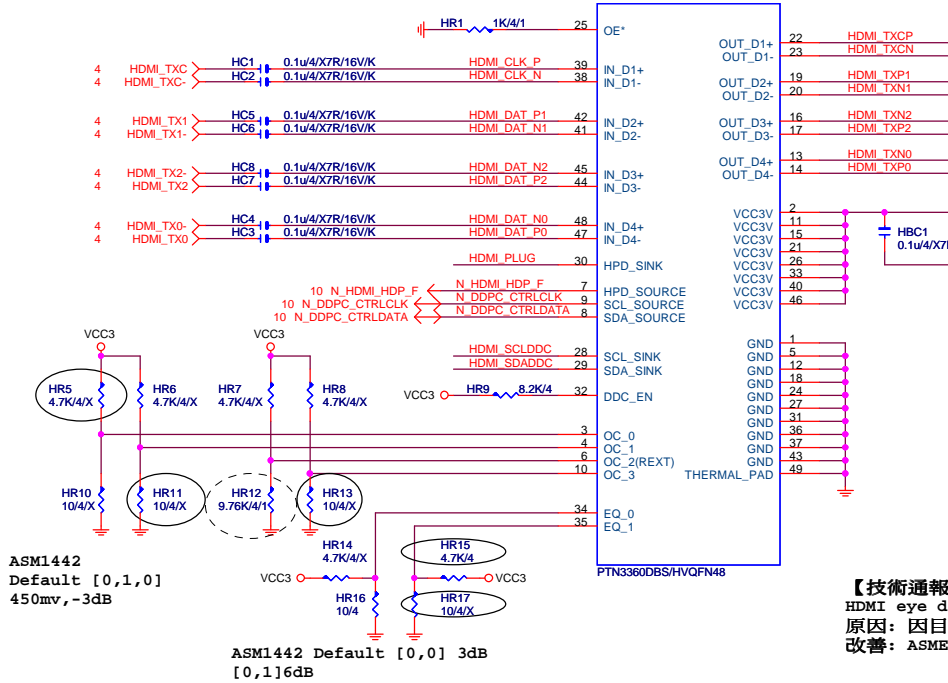
-USB0C_R



Gigabyte Technology			
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HDMI LEVEL SHIFT

HDMI:20/4/6/4/20
Impedance=85 +- 17.5%

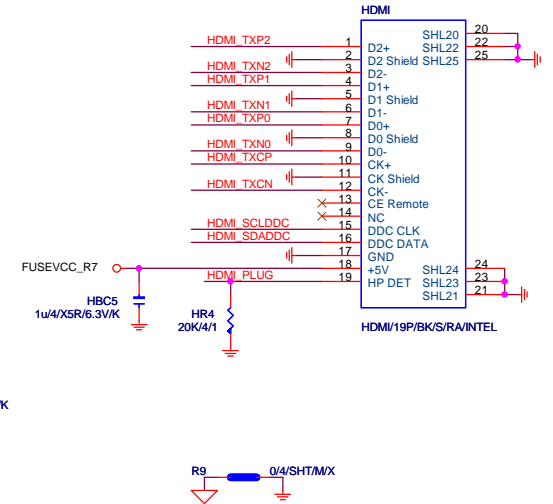
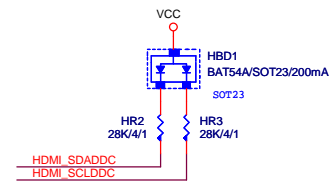


【技術通報R&D技術通報150】

HDMI eye diagram1.4版(deep color)會fail

原因：因目前的HDMI訊號過長，造成RISING TIME過慢，而會壓到eye diagram

改善: ASMEDIA ASM1442 : 3.16K(PIN6 PULL DOWN電阻) 10ohm(PIN4 PULL DOWN電阻)



GIGABYTE™

Title	HDMI
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2.0

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